IJFANS INTERNATIONAL JOURNAL OF FOOD AND NUTRITIONAL SCIENCES
ISSN PRINT 2319 1775 Online 2320 7876
 UGC CARE Listed (Group -I) Journal Volume 11, Iss 12, 2022

Reduce Power Quality Problems Owing to Nonlinear Loads in Electric Grid Systems Using Series APF

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ABSTRACT
An essential indicator of an electrical power system's performance is power quality. Furthermore, issues with the utility grid, like voltage harmonics, imbalances, and swells, have contributed to a reduction in the power quality required for important loads. When non-linear loads are present in weak grids, series active power filters (APF) are a crucial tool for addressing power quality problems. When compared to other tactics in the literature, the series active power filter (APF)'s use of voltage feedback from the critical-load-bus enables a control strategy that offers advantages in terms of processing power and performance, but it can also induce injection transformer saturation. This work provides a control technique that combines an additional control loop with important load-bus voltage feedback.

1. INTRODUCTION

The injection transformer's performance is critical to the system's correct operation. This transformer's design is particularly important since it must contend with issues with cost, performance, overrating, saturation, and overheating. DC voltage components, switching harmonics, and fundamental, desired harmonics can all be included in the injected voltage. Incorrect system operation could arise from the injected voltage saturating the transformer due to incorrect transformer design. Overrating the transformer is the solution suggested in the literature to this issue, however doing so raises the system's overall cost and dimensions.

The authors of this work outline a methodical process for designing and figuring out the transformer's voltage rating while accounting for all frequency components. An equivalent fundamental frequency component is computed to account for every component because it is laborious to create a system that takes into account every frequency component. Transformer current is significantly distorted as a result of the magnetizing current, non-linear load current, and filter current. More power loss could result from this than from pure sinusoidal current. A voltage source converter (VSC) is connected in series from the PCC-bus to the cload-bus via an injection transformer in a traditional series APF arrangement. By deriving the basic voltage from the voltage-controlled series APF, the typical ABC frame control technique indirectly supplies pure sinusoidal voltage to the loads. Other control systems convert sinusoidal to dc variables by using the dq0 reference frame and transformation to distinguish the positive and negative sequences. However, the reference frame translation increases computing work and calls for extra filters. When utilizing a coupling transformer with these control techniques, there is no assurance that the load voltage is properly compensated and disturbances caused by the transformer, such as voltage drops in the leakage inductance, are eliminated if the feedback voltage is placed on the converter side (henceforth referred to as the primary transformer side). Because transformers block dc voltage, if the voltage is monitored at the secondary of the transformer, an undesired dc value at the VSC output would not be observed and might destabilize.

In split capacitor VSC, the controlled dc current is also utilized to provide balanced dc bus capacitor voltage. A three phase inverter with a neutral connection is needed for the series APF in order to correct each voltage independently. The simplest converter to adjust voltage independently in each phase is the three-phase, two-level VSC topology with split dc-bus capacitor.

This topology can be thought of as three separate half-bridge converters sharing a dc-bus. The return path is formed by the neutral conductor.

This allows current to pass between the two capacitors' midpoints, enabling each phase to produce completely independent compensation voltages. Power transfer between phases is made possible by the shared DC bus, allowing phase voltage imbalances to be compensated for. Because the instantaneous current in the neutral conductor is not zero, imbalanced phase voltages in the split capacitor VSC generate ripple in the dc-bus voltage imbalance (voltage differential between the split capacitors). When the dc-bus capacitance is appropriately sized, this is not an issue. Nevertheless, in a constant condition, the neutral conductor current cannot have a dc component because doing so would completely discharge one of the capacitors. An output filter and a split capacitor

3P4W converter make up the suggested series APF. The electrical grid's series APF is connected to the load-bus via three single-phase transformers. The suggested control approach can supply PWM signals to the converter to achieve adequate voltage quality at the cloadbus by monitoring the load voltages (vcl), dc-bus voltages (vdc), and inducer filter currents (if). In order to synchronize the load-bus voltage reference, the PCC-bus voltage (vPCC) is also measured.

2. SYSTEM TOPOLOGY

In Brazil, a three phase transformer that supplies a grounded neutral conductor makes up the standard low-voltage power distribution system. This three-phase, four-wire (3P4W) power system is typically connected to the following loads: office equipment, electric furnaces, lighting ballasts, adjustable speed drives, and other facilities with power electronics. These loads may be single-phase or three-phase, which results in voltage imbalance (different fundamental amplitude) across the three phases. They may also have input current with a high harmonic content, which causes voltage distortion at the PCC.With three independent variables, the distribution line layout creates a non-symmetrical system in which the sum of the phase voltages' instantaneous values might differ from zero.A three-phase inverter with a neutral is needed by the series APF in order to balance each voltage independently.

A three-phase inverter with a neutral connection is needed for the series APF in order to separately correct each voltage. The simplest converter to adjust voltages independently in each phase is the three-phase, two-level VSC topology with split dc-bus capacitor shown in Fig. 1. This configuration can be thought of as three separate half-bridge converters sharing a dc-bus. Each phase can produce completely independent compensation voltages by passing current through the middle of the two capacitors and creating a return channel with the neutral wire.

Phase voltage imbalances can be compensated for by power transfer between phases made possible by the shared dc-bus. Because the instantaneous current in the neutral conductor is not zero, imbalanced phase voltages in the split capacitor VSC might generate ripples in the dc-bus voltage unbalance (voltage difference between the split capacitors). When the dc-bus capacitance is appropriately sized, this is not an issue. But in a stable condition, a dc component in the neutral conductor current is not possible since it would completely discharge one of the capacitors. In order to optimize the output voltage that may be obtained without over-modulation, equal voltages across two capacitors are preferred. For a given maximum capacitor voltage, balanced dc capacitors also optimize the dc bus's energy storage capacity. By adjusting the converter's neutral current, the voltage imbalance can be corrected; however, the neutral current is:

$$i_N = i_A + i_B + i_C,$$

Each phase's dc output current may have a distinct polarity. Transformer saturation results from the neutral dc current being zero and the high dc current having two phases with opposing polarity. In order to achieve dc-bus voltage balance, avoid injection transformer saturation, and independently manage each phase's dc output current, it is therefore preferable to indirectly control the neutral current.

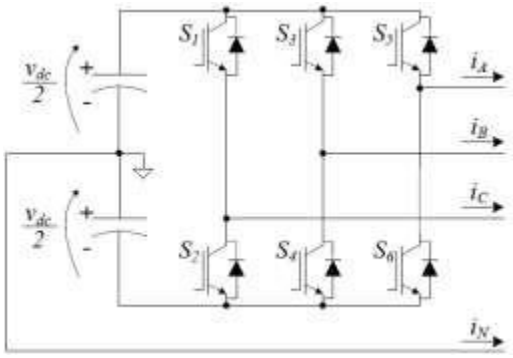

Fig.1.Three-phase,fourwire,splitcapacitorVSC.

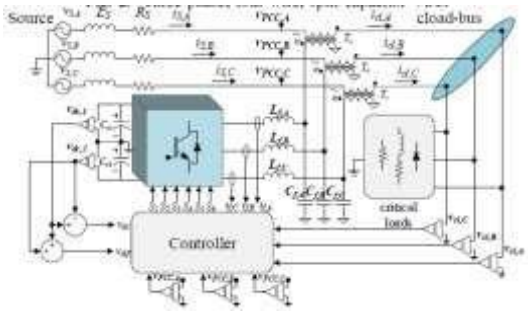

Fig.2.Generaldiagramofthe seriesAPF.

The four leg VSC topology is an additional alternative power circuit design in which the neutral conductor is directly regulated. The fourth leg solution eliminates the requirement for imbalance management and eliminates the need to split the capacitors by adding an extra leg; nevertheless, the complexity and cost of this approach are high because it needs additional switching elements in addition to a controller for the fourth leg. Furthermore, the control of phase dc output current suggested in this study is still necessary in order to prevent the problem of dc output current saturating the transformers caused by the four-leg VSC topology. Consequently, an output filter and a split

ISSN PRINT 2319 1775 Online 2320 7876
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capacitor 3P4W converter make up the suggested series APF in this work.

As seen in Fig 2. The series APF from the utility grid to the load-bus is connected via three single-phase transformers.For simplicity, no PCC-bus loads are displayed. Through the utilization of inductor filter currents (if), dc-bus voltages (vdc), and cload voltages (vcl), the suggested control approach can furnish the converter with PWM signals in order to attain adequate voltage quality at the cload-bus. In order to synchronize the load-bus voltage reference, the PCC-bus voltage (vPCC) is also measured. Figure 3 shows the block diagram of the suggested control scheme for a 3P4W series APF with split dc-bus capacitors. It is made up of two internal control loops (repeated for each phase), which regulate the dc output current and the load-bus voltage, and two external control loops that regulate the dc-bus total voltage and dc-bus voltage imbalance. Figure 3 shows the block diagram of the suggested control scheme for a 3P4W series APF

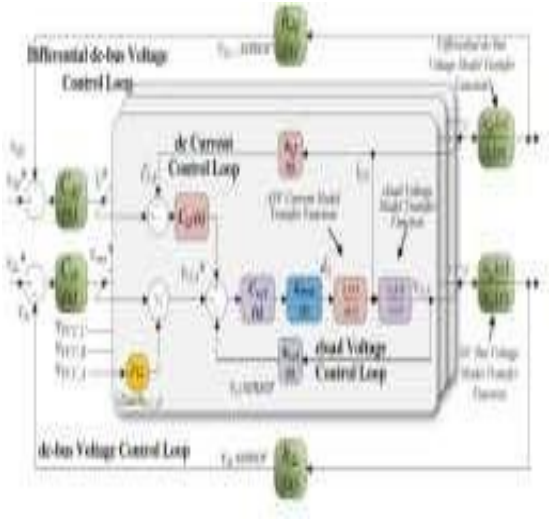

Fig. 3. Block diagram of the series APF controlstrategy including the representation of small signalmodels

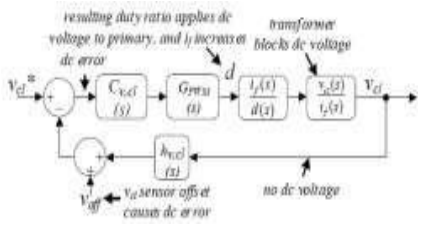

Fig. 4. Example of how cload sensor dc offset cancausedc currentinthe transformer.

The controllers are Cdif for the dc-bus voltage imbalance, Cdc for the total dc-bus voltage, with split dc-bus capacitors. It is made up of two internal control loops (repeated for each phase), which regulate the dc output current and the load-bus voltage, and two external control loops that regulate the dc-bus total voltage and dc-bus voltage imbalance.

The four leg VSC topology is an additional alternative power circuit design in which the neutral conductor is directly regulated. The fourth leg solution eliminates the requirement for imbalance management and eliminates the need to split the capacitors by adding an extra leg; nevertheless, the complexity and cost of this approach are high because it needs additional switching elements in addition to a controller for the fourth leg. Furthermore, the control of phase dc output current suggested in this study is still necessary in order to prevent the problem of dc output current saturating the transformers caused by the four-leg VSC topology. Consequently, an output filter and a split capacitor 3P4W converter make up the suggested series APF in this work..

Cv;cl(s), one for each cload-bus voltage, and Ci;f for each dc output current. Blocks hv;cl, hi;f, hdif, and hdc stand in for sensors, respectively, and indicate the cloadbus voltage, dc output current, dc-bus voltage imbalance,

Block GPWM is used to represent the PWM gain of the inverter. Additionally, small signal models are Used to represent the dc-bus voltage unbalance as a function of dc-output current (Vdif (s)=if (s)), the dc-bus total voltage as a function of load-bus voltage (vdc(s)=vcl(s)), the output current of the inverter (prior to the coupling transformer) as a funct ion of the duty ratio, (if (s)=d(s)), and the load-bus voltage (after the coupling transformer) as a func tion of the output current (vcl(s)=if (s)).With Cv;cl, GPWM, hv;cl, if =d, and vcl=if forming the innermo st control loop, the cload-bus voltage vcl is directly regulated.The dc-bus voltage control loop determines the amplitude of the reference, which is solely sinusoidal and produced by a PLL for the load-voltage controller.

The controller Cv;cl, which tracks the sinusoidal reference by acting on the duty ratio, receives an inaccuracy in its input due to the harmonics in the load voltage. If the branch in the control loop at that point is not taken into

The load-bus voltage loop should not be impacted by the design of the dc-current control loop or the load-bus voltage design. In order to manage the load-bus voltage at line frequency and its harmonics, the converter duty ratio is adjusted by Cv;cl, which simplifies the load-bus control loop. There is also a dc output current control loop in each phase.

This problem cannot be solved by a conventional cascade controller with an inner current loop and an outer voltage loop since doing so would cause the

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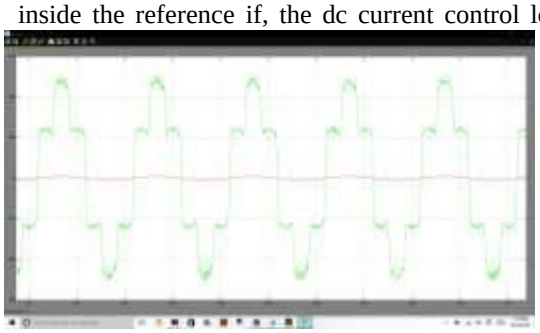
voltage controller to increase the current loop dc reference in an attempt to correct for the voltage offset. This issue is resolved by the suggested control technique in Fig. 3, which modifies the load-bus voltage reference by introducing a compensatory DC voltage. To make sure the dc current on the transformer's primary side stays inside the reference if, the dc current control loop



generates this dc voltage reference. The tiny signal model of the VSC is divided into two sections to enable the design of these control loops: the load-bus and the output current (before the transformer) as a function of the duty ratio.

The whole dc-bus voltage control loop, which is made up of the load-bus voltage control loop, sensor hdc, controller Cdc, and model Vdc=Vcl(s), determines the load voltage's rms amplitude. The voltage drop in the series APF rises with a reduction in the cload voltage, increasing the absorbed active power as well. The absorbed active power decreases when the cload voltage increases, which is the opposite of what happens. The dc-bus charge rate can be adjusted by varying the active power flow into the converter. The sinusoidal voltage references (v_rms) that are received by the three load-bus voltage controllers have the same amplitude. The controllers are able to balance the phase voltages to the same reference with the necessary power thanks to the four wire split-capacitor inverter's ability to create each phase voltage independently.

Fig: 5.SimulationwaveformswithouttheVSC

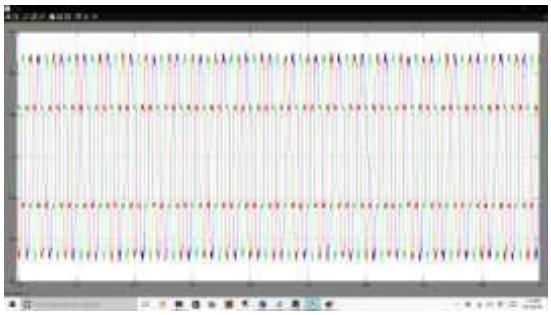


Fig:6.PCC-busvoltagewaveformsoftheseriesAPF

3. SIMULATIONRESULTS

When the system is first operated, the injection transformer is connected and its primary side is shorted, but the series APF VSC is not present. Fig. 5 displays the phase A simulation waveforms. As the dc-bus control approach will raise this voltage drop to compensate for the losses in the series APF VSC, the goal of running the system with the injection transformer is to confirm its series voltage drop.

Fig: 7. Cloud-bus voltage waveforms of the series APF

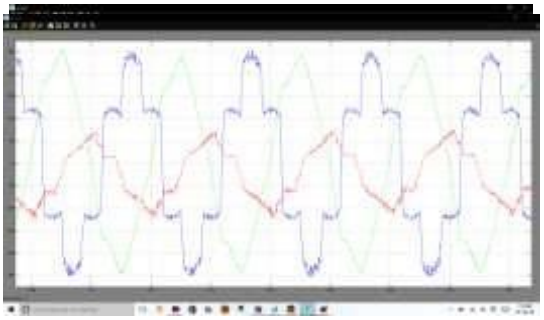


Fig:8. simulation waveforms of phase A cload voltage, PCC voltage, and series APF injected voltage

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