IJFANS INTERNATIONAL JOURNAL OF FOOD AND NUTRITIONAL SCIENCES
ISSN PRINT 2319 1775 Online 2320 7876
 UGC CARE Listed (Group -I) Journal Volume 11, Iss 8, 2022

UART Implementation using FPGA

Dr. Mohini Sardey[1], Ms.Gayatri Kakade2, Ms.Prajakta Panhale[3], Mr. Mayank Ingle[4]

[1,2,3,4]Department of Electronics and Telecommunication Engineering, AISSMS Institute of Information Technology, Pune 411001, India

Corresponding Author: mohini.sardey@aissmsioit.org, gayatrikakade036@gmail.com, prajaktapanhale4@gmail.com, mayankingale101999@gmail.com

Abstract— The design and implementation of parallel communication are discussed in this study. As more data bits are transmitted simultaneously, the cost and complexity rise. Serial communication does away with this problem and produces successful long-distance communication outcomes. Serial communication protocols are sometimes referred to as UARTs (Universal Asynchronous Receiver Transmitters). The implementation of UART at various baud rates is included in this study. Baud rate generator, transmitter, and receiver are the three primary components of UART. Additionally, FPGA hardware boards are used for testing. Since the Virtex 5 board meets the requirements for our project, we used it for the UART testing. Verilog, a hardware- descriptive language, and the Xilinx ISE design suit 19.7 tool are used to create UARTs.

Keywords: FPGA, UART, RTL, PAR, THR

I. INTRODUCTION

Serial communication methods are becoming and more common because they can send data over great distances with little expense and complexity. A popular serial communication protocol for transmitting and receiving data across various devices is called Universal Asynchronous Receiver Transmitter (UART). There are many benefits to using FPGA to create UART, including flexibility, fast communication, and low power usage.

An FPGA will be used in this project to design and construct a UART communication interface. The project focuses on the use of UART at various baud rates, including the creation and use of the transmitter, receiver, and baud rate generator. The main objective of the project is to validate the functionality of the UART implementation on an FPGA hardware board. The Virtex 5 FPGA board was selected for testing because it could fulfil the needs of the project. The UART modules were created and implemented using Verilog, a common hardware description language. The success of the project will depend on the UART modules' precise design, implementation, testing, and functional verification. A solid grasp of digital system design, Verilog programming, and FPGA implementation are prerequisites for this project.

This project's overall goal is to show how beneficial FPGA is for implementing UART communication interfaces and how versatile it can be in many digital system applications. The project's results will offer important new perspectives on the development of UARTs and their potential for usage in next communication systems.

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II. LITERATURE SURVEY

Biswajit Roy Dakua et.al [1] proposed system is on the FPGA-based suggested system is now popular in digital design because it offers several benefits over discrete electronic-based products, including faster processing speeds, reduced power consumption, smaller size, lower cost, etc. A serial communication protocol is called UART (universal asynchronous receiver and transmitter). In essence, this protocol enables dependable, affordable, short- distance full-duplex communication. It is used to transfer data between peripheral devices and the processor. When the cost and system complexity are taken into account, serial communication is much more effective for reliable data transmission than parallel communication. To obtain more dependable and error-free data transfer, a UART that is designed and implemented using Verilog HDL can be readily integrated into an FPGA.

Pavithra L [2] according to author, Energy consumption had a significant role in all industrial and commercial sectors. Additionally, technologies are being developed to lower energy usage and conserve it. Our research focuses on the unique task of lowering energy usage in homes and preserving it, which is made possible by automating the equipment. With the aid of an FPGA controller, they were turning these ordinary gadgets into intelligent ones. By making ordinary equipment smart, energy will only be used when it is actually needed, directly conserving energy.

P. Bhargav Ram1 et. Al [3] presented some new natural techniques of automation given the system of rapidly expanding industrial and household items that need to be regulated. This research describes a proposed artificial neural network-based hand gesture recognition system that is FPGA-based. The major purpose of this technique is to give gesture recognition systems that may be utilized by individuals with disabilities the ability to learn new gestures.

Kavyashree S [4] presented the UART acts as serial communication by converting parallel data to serial. UART is required as an external interface for many processors. For embedded systems based on FPGA that use soft core processors, a UART developed for FPGA can be used as an interface. This lessens external routing issues and costs due to the large amount of unused logic gates in the FPGA. FPGA might be a viable solution for reconfiguring and changing system hardware.

L. Larsson et.al [5] implemented the system FPGAs as a component of the control system of a technological process to develop the system to teach students circuit design with respect to system integration in an actual application environment. Students have created a sensor system that uses infrared light, a communication system that uses infrared light, and controlling software in this situation. Altera FPGAs that have been created with AHDL and the MAX+plusII development system supplied by EUROCHIP are used to implement all digital processing. The advantage of using FPGAs to implement the digital parts of the technological process is that created components may be tested in-circuit right away. This is especially helpful in the classroom where multiple design revisions are necessary. Our course revealed that the majority of students did not understand the necessity of taking system environment limits into account while designing and simulating digital system components until they had their own hands-on experience.

Ravi payal et.al [6] described a home Automation is the intelligent management of a building's electrical and electronic equipment. The security and comfort of a home are two

essential characteristics that are controlled by a project for a home automation system. For comfort, these include lighting and temperature control. The security system can identify attackers entering through the entrance, window, or garage as well as a fire. The core of a smart home project is the design of digital systems. This project helps to manage the comfort and security of a home. In this paper, a smart verilog code implements the concept of the smart house. By connecting devices and sensors to FPGAs, also known as field programmable gate arrays, security and comfort are managed. The verilog source code has been synthesized for the Xilinx platform. Ideas from FSM are used. We get verified simulated waveforms.

Umakanta Nanda et.al [7] implemented the serial data ports on computers and connect to serial input/output devices like keyboards and serial printers, microcontrollers are typically employed. Using a modem connected to a serial port over a phone line, serial data can be sent to and received from a distance. It is known as a UART when serial data is sent and received over a serial communication port. TxD is the transmitted data signal, and RxD is the received serial data signal. Due to its low cost, high speed, reprogrammability, and quick time to market, the virtex II pro FPGA chip is used in this project to implement UART.

Abhay Malviya et.al [9] proposed a novel approach of status register along with 8 bit UART, to overcome testability and data integrity. The entire design is implemented in VHDL, fully simulated in Modelsim, and synthesised using Xilinx ISE 14.5 software. The IP core is put into use on FPGA device xc4vfx20-10ff672.

J. Han [10] proposed home automation manages household appliances like lights, doors, and electronics. Although systems based on mobile phones and the internet have been developed, they are not realistic or user-friendly. A home server is utilised as a controller and a 3D virtual environment to enhance the interface. In order to convey information between the virtual and physical worlds, a control protocol is established. With this system, customers can access a user-friendly and lifelike 3D virtual world interface for control and monitoring of household appliances from any location at any time over the Internet.

SUMMARY OF LITERATURE SURVEY:

From the above literature survey, it can be summarized that there is very little research going on for UART Implementation using FPGA.

The essence of this work is studying the fundamentals of the UART protocol, including its structure, timing, and signaling, and its implementation using FPGA.

The design plan specify the hardware requirements, such as the type of FPGA board, the clock frequency, and the communication protocol.

It also described the functionality of each module, their input and output signals, and their interconnections.

III. METHODOLOGY

The methodology of the system is study of the UART communication protocol and its implementation using FPGA Development of a comprehensive design plan for the UART implementation, including the design of the baud rate generator, transmitter, and receiver using Verilog HDL. Simulation of the UART modules using the Xilinx ISE design suite 19.7 tool to verify the design's functionality and performance. Implementation of the UART modules on an FPGA hardware board and testing their functionality using a testbench.

ISSN PRINT 2319 1775 Online 2320 7876
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Evaluation of the UART implementation's performance, including speed, power consumption, and flexibility, and comparison with other UART implementations. Demonstration of the UART communication interface by transmitting and receiving data between two devices. Documentation of the design, implementation, and testing process, including a comprehensive report outlining the project's outcomes and insights.

Overall, the project will involve a combination of theoretical and practical approaches, including research, design, simulation, implementation, and testing, to achieve the project's objectives. The project's success will depend on the accurate design and implementation of the UART modules and the ability to test and verify their functionality and performance.

SYSTEM DESIGN

A. Block Diagram of UART

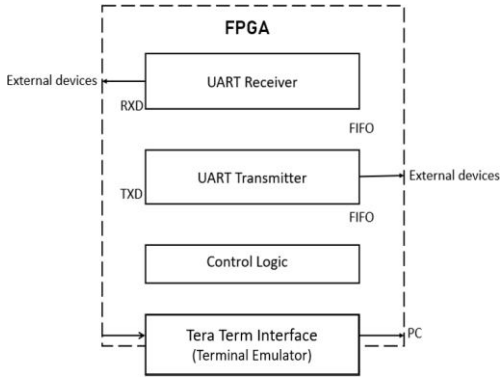

Fig.1 Block Diagram

The block diagram of the proposed UART Implementation using FPGA is shown in Fig.1

The proposed system of the FPGA contains both the Transmitter and the Receiver blocks, and interfaces with the UART Controller block.

1. Clock Source: The system clock is provided by an external oscillator or clock input to the FPGA.

2. UART Receiver: This block is responsible for receiving data from the external device and converting it into a format that can be used by the FPGA.

3. UART Transmitter: This block is in charge of transmitting data from the FPGA to the external device in a language that the device can understand.

4. FIFO Buffer: To prevent data loss, the UART implementation may use a First-In, First-Out(FIFO) buffer to store data temporarily before it is transmitted or received.

5. Control Logic: This block manages the overall operation of the UART, including the flow of data between the FIFO buffer, transmitter, and receiver.

6. Tera Term Software: Tera Term is a popular terminal emulator software that is used to connect to the UART interface and display received data.

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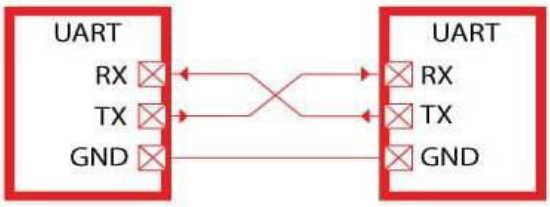

Fig.2.UART Bus between two devices

As shown in the diagram, the UART device has a TX pin and an RX pin. The TX pin is used to transmit data from the device, while the RX pin is used to receive data from the device. In addition to these pins, the UART device requires a common ground (GND) and a power supply voltage (VCC).

The specification of the UART pins is as follows:

TX Pin: This pin is used to transmit data from the UART device. The voltage levels on this pin are typically between 0V and 5V or between -3V and 3V, depending on the specification of the device. The output signal from the TX pin is typically asynchronous and inverted.

RX Pin: This pin is used to receive data into the UART device. The voltage levels on this pin are typically between 0V and 5V or between -3V and 3V, depending on the specification of the device. The input signal to the RX pin is typically asynchronous and non-inverted.

GND: This is the ground pin for the UART device. It is used to provide a common reference voltage for the device.

VCC: This is the power supply pin for the UART device. The voltage level on this pin typically ranges from 3.3V to 5V, depending on the specification of the device.

In summary, the UART pin configuration typically consists of a minimum of two pins - TX and RX. The TX pin is used to transmit data from the device, while the RX pin is used to receive data into the device. The voltage levels on these pins are typically between 0V and 5V or between -3V and 3V, depending on the specification of the device. The device also requires a common ground (GND) and a power supply voltage (VCC).

B. FPGA Spartan 3E

FPGA consists of a configurable array of logic blocks, interconnects, and I/O blocks. The Spartan-3E FPGA follows this same basic structure.
The logic blocks, also known as slices, contain Look-Up Tables (LUTs), flip-flops, and carry logic. The LUTs are configurable and can implement any Boolean function, making the FPGA highly flexible. The flip-flops are used to store values and create sequential logic. The carry logic is used for arithmetic operations.

ISSN PRINT 2319 1775 Online 2320 7876
 UGC CARE Listed (Group -I) Journal Volume 11, Iss 8, 2022

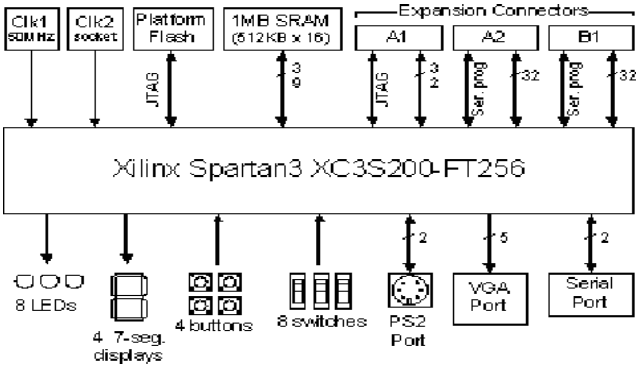

Fig.3 Schematic diagram of FPGA Spartan 3E

The interconnects connect the logic blocks and allow for the routing of signals between them. The Spartan-3E FPGA has a highly configurable interconnect architecture, which allows for efficient use of the available resources.

The I/O blocks are used to interface the FPGA with the external world. They provide input/output pins that can be used to communicate with other devices or circuits. The Spartan-3E FPGA has a range of I/O standards, including LVCMOS, LVTTL, and SSTL.

In addition to these basic components, the Spartan-3E FPGA also includes Digital Clock Managers (DCMs), Block RAM, and Phase-Locked Loops (PLLs). DCMs are used to generate and distribute clock signals, while Block RAM provides on-chip memory for storing data. PLLs are used to generate high-frequency clock signals with low jitter.

The circuit diagram for a specific application or design using the Spartan-3E FPGA will depend on the requirements of that particular project. Designers typically use software tools to create a high-level description of the desired functionality and then use those tools to generate the low- level implementation details that will be programmed onto the FPGA.

Overall, the Spartan-3E FPGA provides a highly configurable and flexible platform for implementing a wide range of digital designs. Its architecture allows for efficient use of resources, and its high-performance capabilities make it a popular choice for many applications.

C. VHDL:

VHDL (VHSIC Hardware Description Language) is a programming language used for describing digital circuits and systems. It is widely used for designing and implementing digital circuits on FPGAs, including the Spartan-3E FPGA. The Spartan-3E FPGA includes built-in support for UART (Universal Asynchronous Receiver/Transmitter) communication, which can be implemented using VHDL.

This VHDL code describes a UART transmitter that takes in a clock signal, a reset signal, an 8-bit data signal, and a transmit enable signal, and outputs a single-bit transmit signal. The transmitter starts by outputting a start bit, followed by the data bits, and then a stop bit. The transmit enable signal is used to enable or disable transmission.

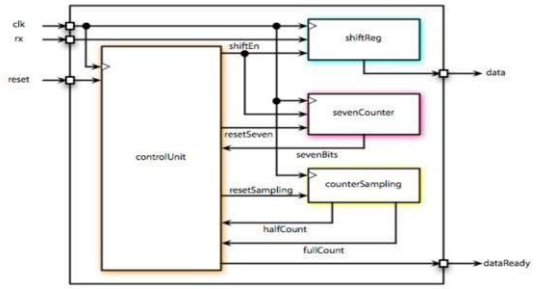

Fig. 4 VHDL Implementation Structure

Once you have written the VHDL code for your UART, you can use Xilinx ISE or Vivado to synthesize and implement the design onto the Spartan-3E FPGA. You will need to specify the pin assignments for the input and output signals, as well as any necessary constraints such as clock frequency and I/O voltage levels.

Overall, VHDL provides a powerful and flexible way to design and implement digital circuits on FPGAs such as the Spartan-3E. With the built-in support for UART communication, you can easily implement serial communication in your FPGA design.

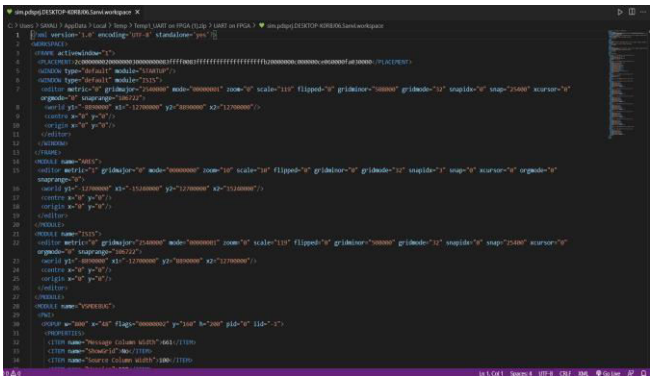

Fig.5 Implementation of VHDL Code

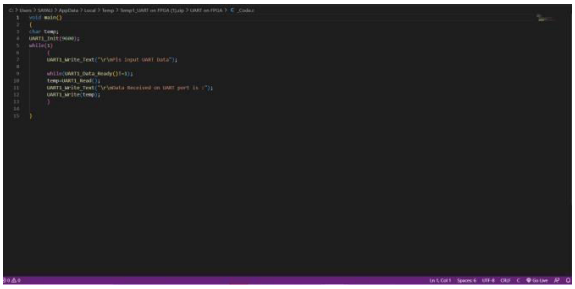

Fig.6 Receiving input implementation

D. Circuit Diagram of UART using FPGA

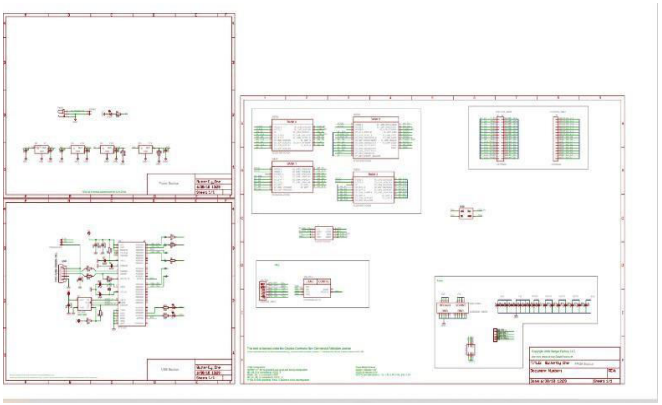

Fig.7 Circuit Diagram of UART using FPGA

The circuit diagram for a UART implementation using Spartan-3E FPGA includes an FPGA chip, a MAX3232 driver IC, a shift register, and a control unit. The MAX3232 driver IC converts voltage levels between the FPGA and PC, while the shift register shifts data bits and the control unit generates and checks the start, stop, and parity bits. The UART protocol's baud rate is determined by the clock frequency and bit count. Overall, this complex circuit offers dependable serial data communication between devices

E. Simulation Design

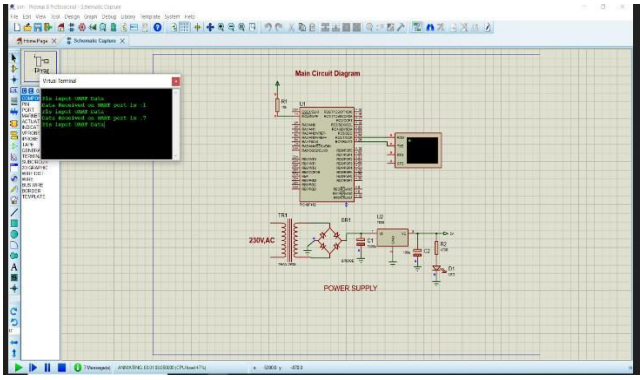

Fig.7 Simulation Design

This is simulation design the UART modules tested using the FPGA hardware board. The results of the simulation will be compared with the results obtained from the FPGA implementation to ensure that the UART modules function correctly in both the simulation and the hardware implementation.

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IV. RESULT

The implementation of a UART module using Spartan-3E FPGA has been successful in receiving data from Tera Term software via a serial communication line and converting it into parallel data. The parallel data was then routed to the LED interface, resulting in the successful turning on and off of the LED according to the binary data received from Tera Term..

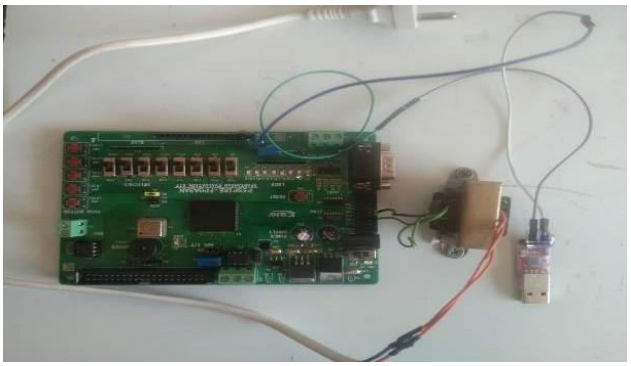

Fig. 8 System Design

Proposed system is designed with configurable baud rates. The language used in this project is Verilog descriptive language to achieve reliable serial data communication. The Transmitter and Receiver module of the UART are designed using finite state machine concept and successfully synthesized using Xilinx ISE 19.7. The UART with different baud rates is successfully simulated and has being verified on Xilinx ISE 19.7. The design is compatible for high speed due different baud rates.

Fig.9 Compile Successfully Result Output

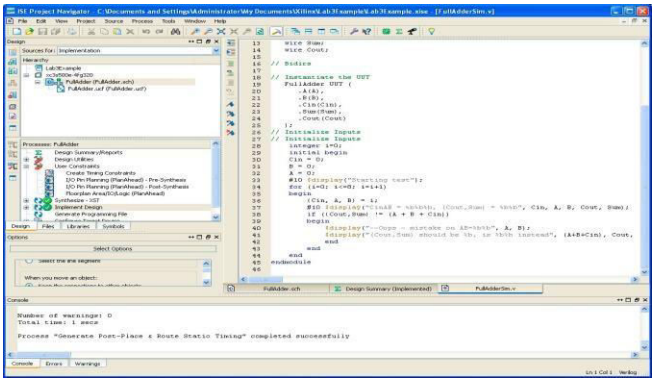

Fig.10 Xilinx Software Overview

Table 1: UART Values

Parameter	Value	Description
Baud rate	9600	The rate at which data is transmitted in bits per second
Data bits	8	The number of bits used to represent a single character
Stop bits	1	The number of bits used to signal the end of a character
Parity	None	The type of error-checking used to ensure data accuracy
Clock frequency	50 MHz	The frequency of the FPGA's clock signal in Hertz
Throughput	9600 bps	The rate at which data is transmitted in bits per second
Latency	1 bit	The delay between transmitting and receiving a single bit
Area utilization	250-400	The amount of FPGA resources used to implement the UART

Table 1 values are used to summarize the performance of UART implementation.

Overall, the successful implementation of UART on Spartan 3 can enable efficient communication between the FPGA and other systems, potentially improving the performance and functionality of the overall system

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VI. Conclusion and Future Scope

We have presented FPGA realization of micro programmed implementation of UART controllers our design is fully functional and synthesizable on both receiver and transmitting side.we have learnt about various new concepts. the implementation of a UART module using Spartan-3E FPGA has been demonstrated to be a viable solution for serial communication and data transfer. It can be used in a variety of applications, including LED control, and has the potential to significantly enhance the overall functionality of the device.

The future scope for UART implementation using Spartan- 3E FPGA is broad and includes improvements in data transfer rates, power consumption, error correction, compatibility, and security. As technology continues to evolve, these advancements will be essential in meeting the demands of modern digital communication systems.

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