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VLSI chip test power reduction using IoT Monitoring.

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Abstract

The main problem with current generation VLSI testing is test power. It has grown to be the SoC's top worry today. The modular design strategy in SoC (i.e., utilisation of IP cores in SoC) has further exacerbated the test power issue while lowering design efforts. It is difficult to choose a successful low-power testing method from a wide range of various techniques that are readily available. In this study, the state of the art in low-power testing is described, starting from the vocabulary and models for power consumption during test, to determine the appropriate solutions for test power reduction approach for IP core-based SoC. The study provides a thorough analysis of the numerous power reduction approaches suggested for all testing aspects, including built-in self-testing procedures, external testing,

Key: VLSI, Chip, Test, Power, Reduction, IoT, Monitoring.

Introduction

Both design and test engineers have found the power consumption to be a significant difficulty. The power consumption issue during testing was made worse by attempts to reduce power consumption in regular operation mode. A circuit may typically use 3–8 times as much power in test mode as it does in regular mode [1]. As a result, low-power testing methods are in demand in the semiconductor sector [2].

The modular design technique is mainly used for SoC in order to save costs and shorten time to market. Such predesigned, usable intellectual property (IP) core frequently conceals its structure from the system integrator. Therefore, evaluating such cores is significantly more difficult. As a result, several limitations are

placed on the current low-power testing methods by the power reduction during testing of such cores. to progress.

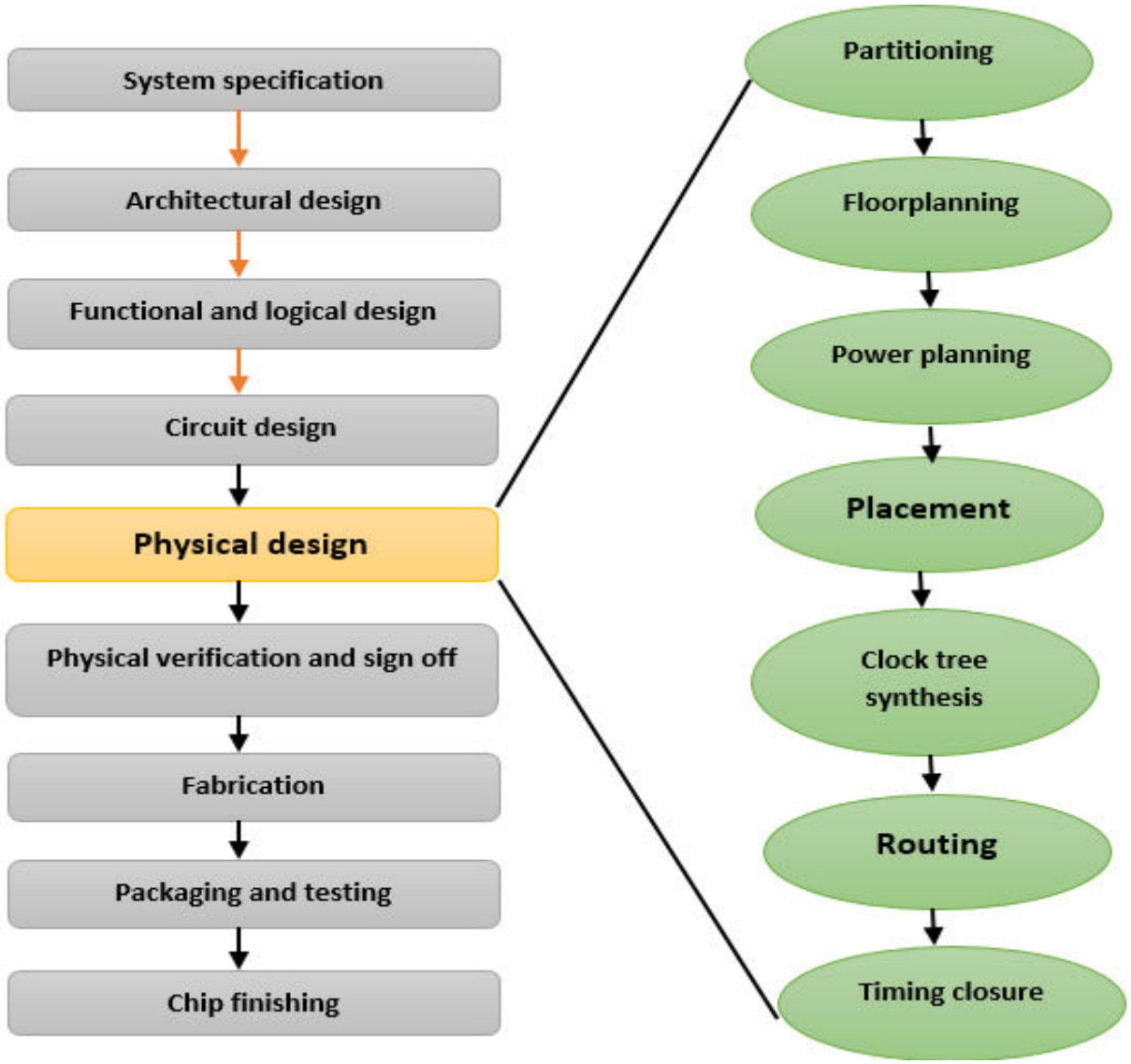

Fig.1: VLSI chip test power reduction using IoT Monitoring Flow.

Low-Power Test

A nondestructive test that satisfies all the power limitations specified during the design phase is always required for a high density system like an ASIC or SoC. The current testing strategy, on the other hand, requires significantly more power usage during testing than during functional mode. The causes and consequences of such high power usage are discussed in this section.

The destruction of the IC itself is the most detrimental result of very high-power dissipation during testing. The power dissipation during testing can also have an impact on cost, reliability, autonomy, performance-verification, and yield-related issues [4].

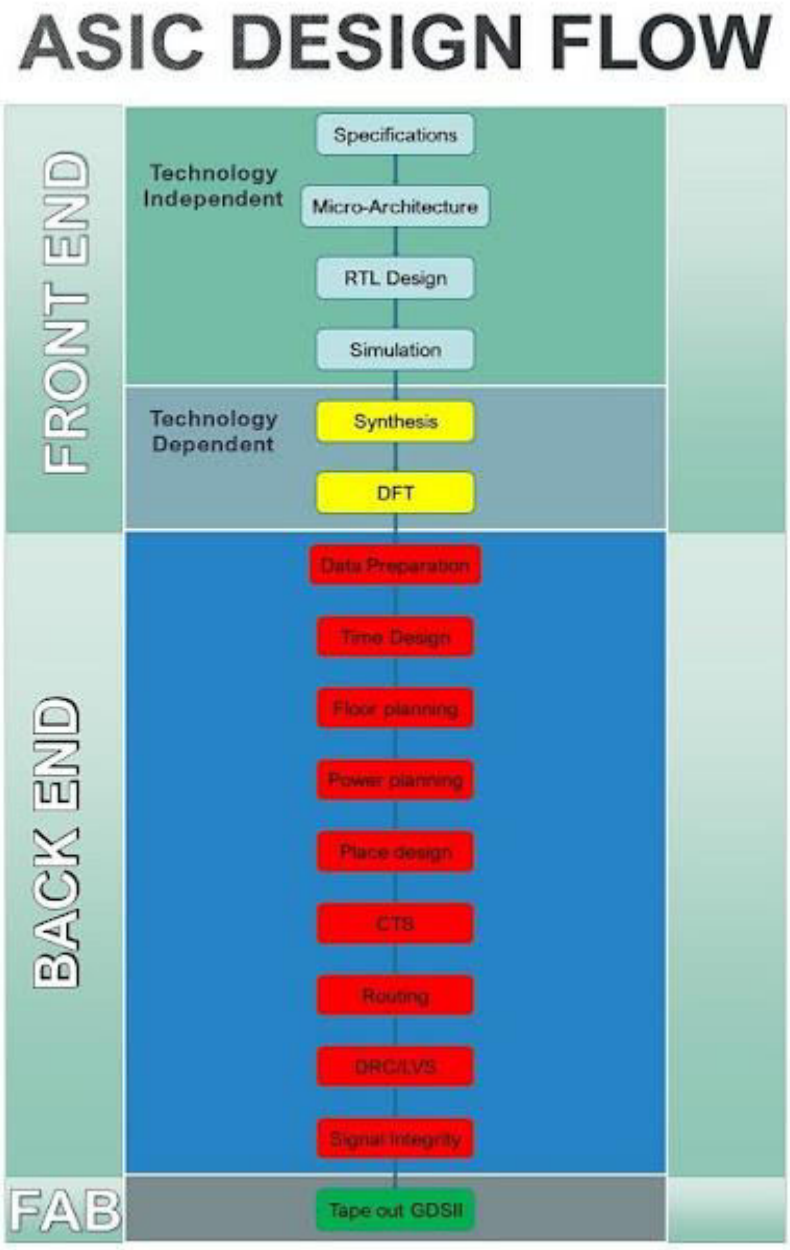

Fig.2: VLSI chip test power reduction using IoT Monitoring Process.

The following are a few of the impacts.(i)Due to the significant power dissipation, the increasing need for at-speed testing may be restricted. Therefore, testing stuck at faults is unaffected, but testing the delay fault will be challenging.(ii)The naked, unpackaged die has extremely little space for power or heat dissipation

during functional testing of the die right after wafer etching. For systems based on multichip module technology, for instance, this might be an issue because designers won't be able to take advantage of the possible gains in circuit density and performance without access to completely verified bare dies [5].(iii) Electromigration-induced conductor degradation can lead to circuit failure.(iv) The battery-operated remotes and portable systems' internet BIST consumes a lot of power solely for testing. Distant system.

Low-Power Testing Schemes

The number of switches a node i makes in the circuit determines the energy, the peak power, and the average power consumption, according to the above expressions for power and energy consumption, assuming a specific CMOS technology and supply voltage for the circuit design. Similar to this, the peak power and average power are affected by the testing clock frequency. Finally, only the overall energy usage is impacted by the test duration and the quantity of test patterns applied to the CUT. Consequently, a designer or test engineer must keep these relationships in mind while coming up with a solution for power and/or energy minimization during test.

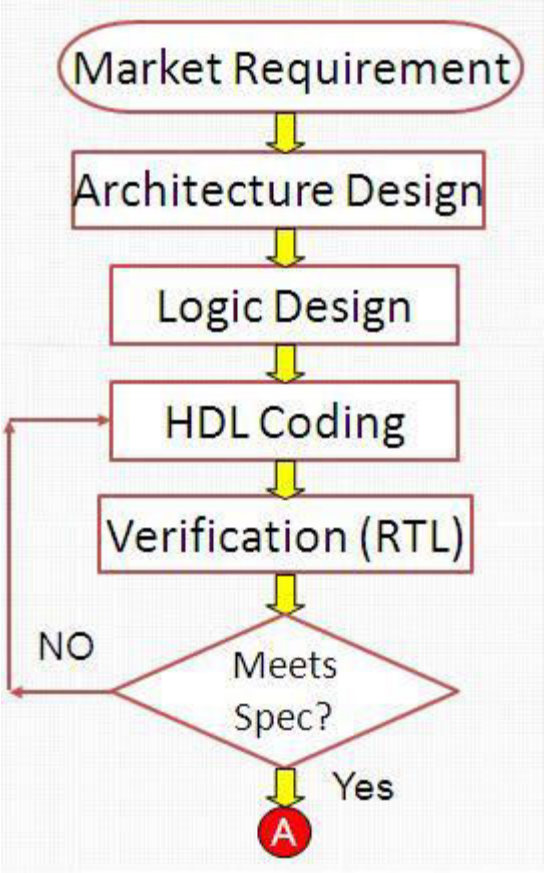

Fig.3: VLSI chip test power reduction using IoT Monitoring. Flow Chart.

Test power can be separated into shift power and capture power, which correspond to shift mode and capture mode, respectively, from the perspective of a scan test. In shift mode, a test vector is loaded and a test response is unloaded using a large number of clock pulses. As a result, heat dissipation during scan shift is dominated by average shift power. Peak shift power that is too high might damage scan chains and reduce yield. The contribution to test heat in capture mode, where only one or two clock pulses are required, is minimal.

The variety of power reduction testing approaches has increased during the past 20 years. These methods either investigate the ATPG and deal with the test vectors for external testing or investigate the internal structure of the design using BIST or DFT. Consequently, the two categories below are used to categorise the current low-power testing scheme.(1) Low-Power Testing Methodologies for External Testing Using ATE, ATPG, etc.(2) Internal Testing with Low Power Techniques Using BIST, DFT, etc.

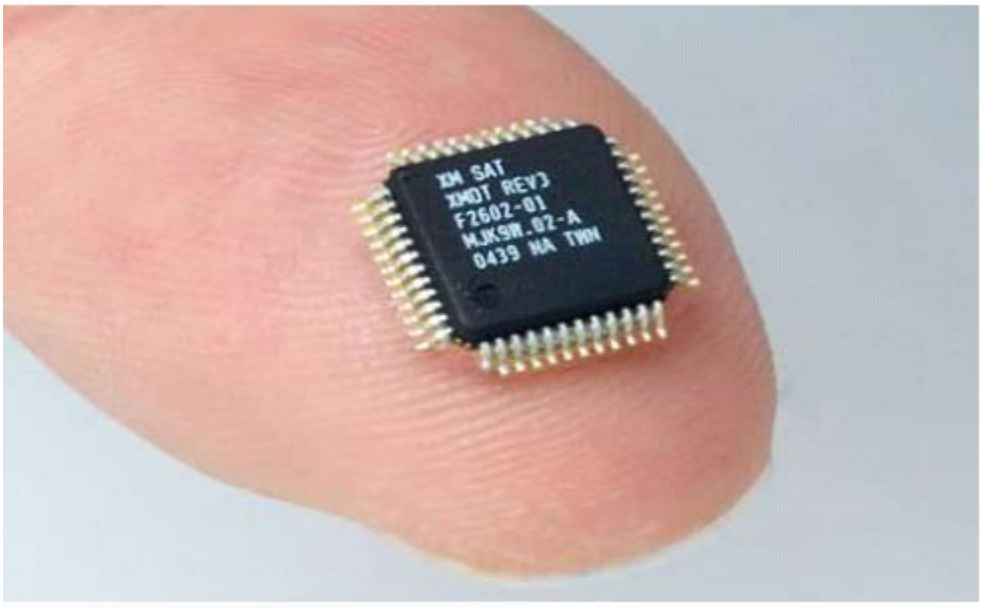

Fig.4: VLSI chip test power reduction using IoT Monitoring.

This higher test power can be attributed to a number of factors. The following are the key causes among them.(i) It has been demonstrated that the toggle rate and test efficiency have a strong association, so during tests all nodes frequently switch more frequently than they do during normal operations.(ii)Parallel testing is typically used in a SoC to shorten test application times, but this may lead to excessive energy and power loss.

(iii) During normal operations, the design-for-testability circuitry embedded in a circuit to lower the test complexity is frequently inactive, but it may be intensively utilised during the test mode.(iv)That while the correlation between successive test patterns can be very low, it is present between successive functional input vectors presented to a given circuit while it is operating in system mode. This could result in a circuit's switching activity and power dissipation during a test being much higher than they would be under normal operating conditions [3].

Low-Power Testing Techniques Emphasizing IP Core-Based SoC

Because it provides for the preservation of a design's intellectual property, BIST, which is already existing as a component of IP core with the emergence of core-based SoC design, presents one of the most advantageous testing methodologies [45]. Such BISTs are most suitable to test the IP core in standalone mode, but, when the IP core is integrated with other blocks to form a complete system, they might not be suitable.

Results

Let's consider incorporating some low-power strategies while integrating the system. System integrators are frequently unaware of the IP cores' structural details. Therefore, IP cores are not capable of modifying their internal scan chain or inserting DFTs. Additionally, it cannot be tested using any testing tools like the Automatic Test Pattern Generator (ATPG) or fault simulation. These cores provide ready-to-use test data.

With the help of this test data, the core may be evaluated both independently and after being fully incorporated into the system. The system integrator's responsibility is to make sure that the logic around the core permits the application of test stimuli and the transportation of created responses for evaluation. Typically, it is considered that the core is directly accessible. The sole remaining option for power reduction is a plan that uses test data that has already been generated.

This category includes numerous methods that ATE has used to cut back on power usage when doing external testing. The number of transitions in the test data set affects how these strategies work. The present study in this area focuses on the ATPG algorithm, which not only ensures the maximum fault coverage at the lowest feasible power dissipation but also delivers the maximum fault coverage. By adding the high- and low-frequency effects using a dynamically limited variant of the traditional D-algorithm for test generation, Reference [6] suggested a heuristic way to build test sequences that produce worst-case power droop.

The shift and capture power can both be decreased while using the current ATPG flows thanks to a novel scan chain division algorithm [7] that analyses the signal interdependence and divides the circuit into several sections. A low capture power ATPG and a power-conscious test compaction approach are presented in Reference [8]. When compared to the detection number n, this ATPG slows the rise of the test

pattern count. As the detection number n rises, the peak power decreases. The average capture power and the number of test patterns are both further decreased by the test compaction technique.

Conclusion

This review article on low-power testing methods appropriate for IP core-based SoCs begins with an analysis of the causes and consequences of excessive test power consumption, including an energy and power model. These extremely sophisticated methods for power reduction during testing are detailed in detail. In the context of IP core-based SoCs, concerns with test power reduction are examined, and characteristics of the optimum scheme are specified. Based on that, this ideal model is contrasted with each category of power reduction that is now available. The best methods for an IP core-based SoC are determined to be "ordering techniques" and "exploring do not care bits" methods. These schemes can be improved in terms of power reduction to start the research, and it can then be further optimised with other crucial test characteristics like test application time, on-chip space overhead, test data compression, and so on.

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