IJFANS INTERNATIONAL JOURNAL OF FOOD AND NUTRITIONAL SCIENCES
ISSN PRINT 2319 1775 Online 2320 7876
 Journal Volume 10, Iss 11, 2021

LOW POWER DELAY BUFFER USING GATED DRIVER TREE

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ABSTRACT:
This paper presents circuit design of a low-power delay buffer. The proposed delay buffer uses several new techniques to reduce its power consumption. Since delay buffer r accessed sequentially, it adopts a ring-counter addressing scheme. In the ring counter, double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half and the C-element gated-clock strategy is proposed. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. Moreover, the gated-driver-tree idea is also employed in the input and output ports of the memory block to decrease their loading, thus saving even more power.

1. INTRODUCTION:

PORTABLE multimedia and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the widespread success of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very important. In many such products, delay buffers (line buffers, delay lines) make up a significant portion of their circuits [1]–[3]. Suchserial access memory is needed in temporary storage of signals that are being processed, e.g., delay of one line of video signals, delay of signals within a fast Fourier transform (FFT) architectures [4], and delay of signals in a delay correlator [2]. Currently, most circuits adopt static random access memory (SRAM) plus some control/addressing logic to implement delay buffers. For smaller-length delay buffers, shift register can be used instead. The former approach is convenient since SRAM compilers are readily available and they are optimized to generate memory modules with low power consumption and high operation speed with a compact cell size. The latter approach is also convenient since shift register can be easily synthesized, though it many consume much power due to unnecessary data movement. Previously, a simplified and thus lower-power sequential addressing scheme for SRAM application in delay buffers is proposed in [5]. A ring counter is used to point to the target words to be written-in and read-out. Since the ring counter is made up of an array of D-type flip-flops (DFFs) triggered by a globalclock signal and all except one DFFs have a value of “0,” it is possible to disable the clock signal to most DFFs. Such a gated-clock ring counter is implemented in [6] to compose a low-power first-in–first-out (FIFO) memory. The skyrocketing increasing transistor count and circuit density of modern very large scale integrated (VLSI) circuits have made them extremely difficult and expensive to test

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 Journal Volume 10, Iss 11, 2021

comprehensively. The DFT method In a digital processing chip of mobile communications, the delay buffer takes up a large portion of the circuit layout. If the power consumption of the delay buffer could be reduced significantly, the overall power consumption of the digital processing chip could be reduced significantly as well. On the other hand, as these chips are working at even higher operation frequencies, a new, lowpower delay buffer should be operable under high frequencies. Within parentheses, following the example. Some components, such as multi-leveled equations, graphics, and tables are not prescribed, although the various table text styles are provided. The formatter will need to create these components, incorporating the applicable criteria that follow. In today's electronics, delay buffer plays a crucial role when data is shifted from one memory array or processor (sender) to another memory array or processor (receiver). SRAM are used to implement this delay buffer when control and addressing line is added. Recently three primary technologies have been used in building memory hierarchies. Main memory uses Dynamic Random Access Memory (DRAM), whereas cache uses SRAM. Even though DRAM is slower, it is costly then SRAM, because less area is used by DRAM. Buffers are created with different method. If the buffer length is shorter SISO shift register is used for addressing the memory. Since, 64*8 memory is a long buffer memory, it has been implemented using ring counter method for the address generation process. Then the ring counter is modified with octa and octaX2 gated clock forreducing power consumption. In this paper the proposed SRAM with the base of ring counter and ADPLL technique is to be employed. ADPLL will reduce the size of buffer by tuning the transmitter clock frequency in reference with receiver clock frequency. Previously, a simplified and thus lower-power consecutive addressing theme for SRAM application in delay buffers is planned in [5]. A ring counter is utilized to purpose to the target words to be written-in and read-out. Since the ring counter is created from associate array of D-type flip-flops (DFFs) triggered by a global clock signal and everyone except one DFFs have a value of "0," its potential to disable the clock signal to most DFFs. Such a gated-clock ring counter is enforced in [6] to compose a low-power first-in–first-out (FIFO) memory. Nowadays, the area occupied by embedded memories in System-on-Chip (SoC) is over 90%, and expected to rise up to 94% by 2015. As those memories are very tightly integrated with large number of transistors causes 90% of overall faults in system on chips Thus, they concentrate the large majority of defects. In addition, with aggressive nanometer scaling, defect types are becoming more complex and diverse and may escape detection during fabrication test. If they are not treated adequately, the above trends will increase defect level, affect circuit quality dramatically and impact reliability, as undetected fabrication faults will be manifested as field failures. To cope with, the ability to guaranty a high quality

test should be integrated in memory BIST, which is the mainstream test technology for embedded memories. Memory BIST generators can integrate a limited set of test algorithms (see for instance [1][2][3]). Thus, only the test algorithms selected during the design phase can be used after fabrication. However, fixing the memory test algorithms during the design phase is not a good strategy as unexpected failures may be discovered after production. Also, integrating pre-emotively a large number of test algorithms in the BIST generator will result in large area cost. Thus, programmable memory BIST enabling selecting the memory, y test stimuli in silicon and testing the memory for a wide variety of faults is becoming mandatory. This flexibility has to be achieved at low area cost, to make the approach attractive for real products. Also, the flexibility offered by programmable BIST is highly important for thorough screening inspection, failure analysis of customer returns, debug of a new fabrication process or a new memory design, and production ramp-up, since the most challenging issue in these processes is to detect and/or diagnose unexpected failures.

There are three memory test stimuli components: the test algorithm determining the operations performed in each memory cell and the instances they performed; the data used in these operations; and the sequence in which the memory addresses are visited by the test algorithm. Previous work comprises programmable BIST enabling test algorithm programmability [4-8] and data programmability [7][9], but no previous work exist concerning address sequence programmability. In the present paper we extend programmable BIST to incorporated address sequence programmability in addition to test algorithm programmability and test data programmability. Thus, all the components of memory test stimuli could be programmed in silicon, enabling testing unexpected failures during fabrication go/no go test, as well as comprehensive testing and diagnosis during failure analysis of customer returns; debug of new fabrication process or new memory design; and production ramp-up. The main challenge when implementing complete programmability of the address sequence used concerns the large amount of data that have to be programmed (here the complete memory address space) and the associated high hardware cost. We resolve this problem by adapting the transparent BIST scheme [10-16] in a way enabling storing the address sequence in the memory under test and using it for testing the memory. This paper talks about walking, marching and galloping pattern tests for RAM. Random access memory circuits are among some of the highly dense VLSI circuits that are being fabricated today. Since the transistor lines are very close to each other, RAM circuits suffer from a very high average number of physical defects per unit chip area compared with other circuits. This fact has motivated researchers to develop efficient RAM test sequences that provide good fault coverage. For testing today's high density memories traditional algorithms take too much test time. For instance GALPAT and WALKING I/O

[5][6] require test times of order n^2 and $n^{3/2}$(where n is the number of bits in the chip). At that rate, assuming a cycle time of 100 ns, testing a 16Mbit chip would require 500 hours for an n^2 test and 860 seconds for an order $n^{3/2}$ test. Other older tests, such as Zero-One and Checkerboard, are of order n, but they have poor fault coverage. Due to the rapid progress in the very large scale integrated (VLSI) technology, an increasing number of transistors can be fabricated onto a single silicon die. For example, a state-of-the-art 130 nm complementary metal-oxide semiconductor (CMOS) process technology can have up to eight metal layers, poly gate lengths as small as 80 nm and silicon densities of 200K-300K gates/mm2 [37]. However, although milliongates integrated circuits (ICs) can be manufactured, the increased chip complexity requires robust and sophisticated test methods. Hence, manufacturing test is becoming an enabling technology that can improve the declining manufacturing yield, as well as control the production cost, which is on the rise due to the escalating volume of test data and testing times. Therefore reducing the cost of manufacturing test, while improving the test quality required to achieve higher product reliability and manufacturing yield, has already been established as a key task in VLSI design [8]. Embedded Memories are growing rapidly to a large amount in terms of its size and density. As Embedded memories are using complex design structures the chances of occurring manufacturing defects is more compared to any other embedded core on SOC. Hence testing of embedded memory is a real challenge for design architect. For SOC the inability to have direct access to a core is one of the major problems in testing and diagnosis .Further the available bandwidth between the primary inputs of the system chip and the embedded core is usually limited. Hence the external access for test purpose is often infeasible. This has prompted a very strong interest in self test of embedded arrays. In particular, functional March tests have found wide acceptance, mostly because they provide defined detection properties for classical memory array faults such as stuck at faults and transition faults. Memory tests are used to confirm that each location in a memory device is working. This involves writing a set of data to each memory address and verifying this data by reading it back. If all the values read back are the same as those that were written, then the memory device is said to pass the test, otherwise device fails. Different test methodologies have been evolved from the years to identify the memory defects, one such test is memory built in self test which involves built in self test circuitry for each memory array.

The advantage of March tests lay in the fact that high fault coverage can be obtained and the test time were usually linear with the size of the memory which makes it acceptable from industrial point of view. March based algorithms were capable of locating and identifying the fault types which can help to catch design and manufacturing errors. Especially SAF dominate the majority of defects that occur

in embedded RAMS. Due to the rapid progress in the very large scale integrated (VLSI) technology and large number of transistors can be fabricated onto a single silicon die. Although million gate the increased chip complexity requires robust and sophisticated test methods. Hence, manufacturing test is becoming an enabling technology that can improve the declining manufacturing yield, as well as control the production cost, which is on the rise due to the escalating volume of test data and testing times. Therefore reducing the cost of manufacturing test, while improving the test quality required to achieve higher product reliability and manufacturing yield, has already been established as a key task in VLSI design.

2. LITERATURE SURVEY:

Many of the methods used to interface clock domains within an integrated circuit use an asynchronous wrapper around synchronous blocks which alters the local clock of the synchronous logic [2]. Gated-clock ring counter [6] is implemented in to compose a low-power first-in–first out (FIFO) memory. The EMPTY (STRETCHED) output stops the external decision-making logic from making Read Clock go High [7]. EMPTY (STRETCHED) therefore, stays active even after data has been written into the FIFO. FULL (STRETCHED) would behave similarly without a free running Write Clock. Free-running clocks, activated by their respective enable signals, avoid these problems. The two most significant bits of both counters are compared, since they indicate in which quadrant of the 16-position circular address space the present address resides. These two most significant bits of both address counters together are used to address two 4-input look-up tables in parallel. The look-up tables (LUTs) [9, 10]decode the relative quadrant position of the two counters. The 4-bit LUT address describes one of 16 possible conditions. The need for large data transfer from/to mass storage in multiprocessing and data communication fields has become more critical in recent years. Data transfer speed is becoming a bottleneck in these systems and the necessity for large data buffers is widely recognized. Mainframe systems have started to implement expanded storage or semiconductor disks within the system to improve its speed performance. Since the system simplicity is an essential factor in the expanded storage, FIFO memory is believed to be one of the best configurations. Simple controllability also makes FIFO memory most suitable for consumer products. The proposed encoding scheme acted as the second stage of compression after LFSR reseeding. It accomplished two goals: first, it reduced the number of transitions in the scan chains by filling the unspecified bits in a different manner; second, it reduced the number of specified bits that need to be generated via LFSR reseeding. Experimental results indicated that the proposed method significantly reduced test power and in most cases provides greater test-data compression than LFSR reseeding alone (Wang and Gupta, 1997) proposed an optimization

algorithm for low power design methodologies, which was able to explore the trade-off between low power and high testability. The algorithm was based on a newly proposed power estimation function, and on an estimate of the expected test length of a pseudo-random test session. The algorithm was experimentally shown the power and area optimization in favour of testability improvement. (Tehranipoor et al., 2005) proposed a low transition TPG, called LT-LFSR, to reduce average and peak power of a circuit during test by reducing the transitions within random test pattern and between consecutive patterns.

3. DIGITAL BUFFER

Digital Buffers and Tri-state Buffers can provide current amplification in a digital circuit to drive output loads

In a previous tutorial we looked at the digital not gate commonly called an inverter, and we saw that the NOT gates output state is the complement, opposite or inverse of its input signal.

So for example, when the single input to NOT gate is “HIGH”, its output state will NOT be “HIGH”. When its input signal is “LOW” its output state will NOT be “LOW”, in other words it “inverts” its input signal, hence the name “Inverter”.

But sometimes in digital electronic circuits we need to isolate logic gates from each other or have them drive or switch higher than normal loads, such as relays, solenoids and lamps without the need for inversion. One type of single input logic gate that allows us to do just that is called the **Digital Buffer**. Unlike the single input, single output inverter or NOT gate such as the TTL 7404 which inverts or complements its input signal on the output, the “Buffer” performs no inversion or decision making capabilities (like logic gates with two or more inputs) but instead produces an output which exactly matches that of its input. In other words, a digital buffer does nothing as its output state equals its input state. Then digital buffers can be regarded as Idempotent gates applying Boole’s Idempotent Law because when an input passes through this device its value is not changed.

MEMORY ORGANIZATION:

This section describes PJMEDIA's implementation of delay buffer. Delay buffer works quite similarly like a fixed jitter buffer, that is it will delay the frame retrieval by some interval so that caller will get continuous frame from the buffer. This can be useful when the operations are not evenly interleaved, for example when caller performs burst of put() operations and then followed by burst of operations. With using this delay buffer, the buffer will put the burst frames into a buffer so that get() operations will always get a frame from the buffer (assuming that the number of get() and put() are matched).

The buffer is adaptive, that is it continuously learns the optimal delay to be applied to the audio flow at run-time. Once the optimal delay has been learned, the delay buffer will apply this delay to the audio

ISSN PRINT 2319 1775 Online 2320 7876
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flow, expanding or shrinking the audio samples as necessary when the actual audio samples in the buffer are too low or too high.

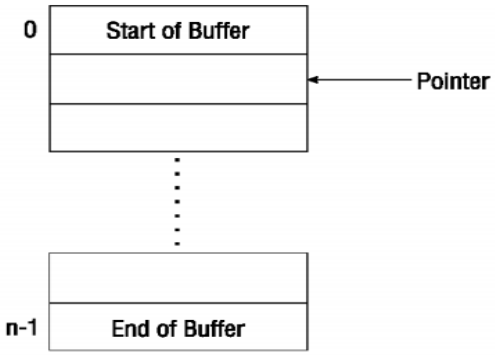

Fig :1. Buffer

TECHNIQUE:

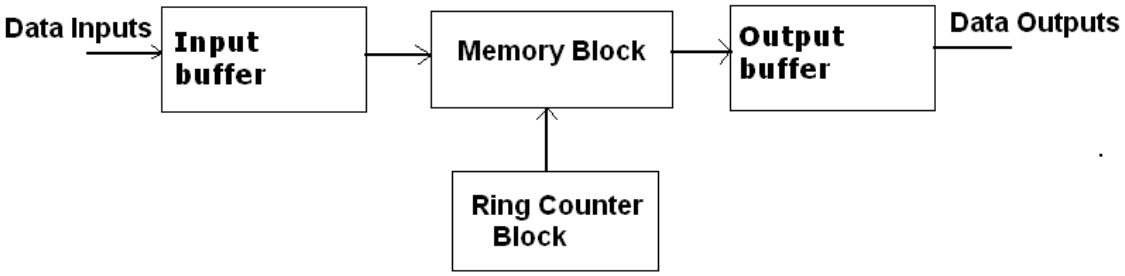

Fig :2. Existing Block Of Memory Organisation

4. PROPOSED DELAY BUFFERS

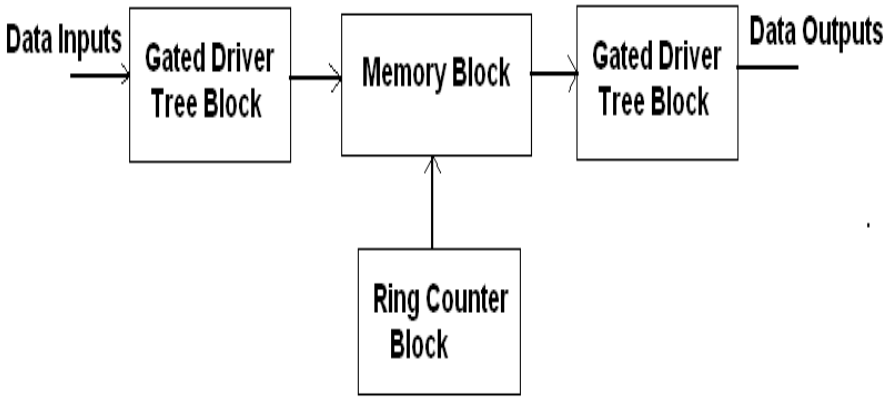

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Fig 4.1: Block Diagram For Proposed Delay Buffer

4.1 GATED DRIVER TREE:

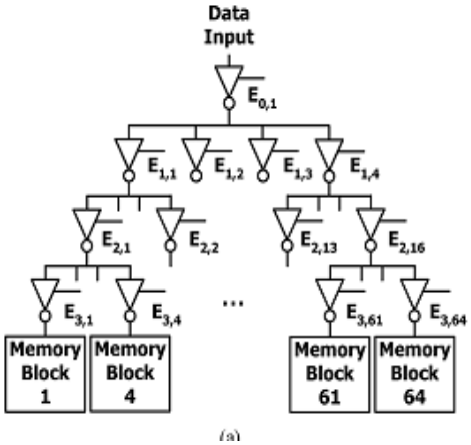

Fig 4.2: Gated Driver Tree

Gated driver tree derived from the same clock gating signals of the blocks that they drive. Thus, in a quad-tree clock distribution network, the "gate" signal of the gate driver at the level (CKE) should be asserted when the active DET flip-flop

4.2 MODIFIED RING COUNTER:

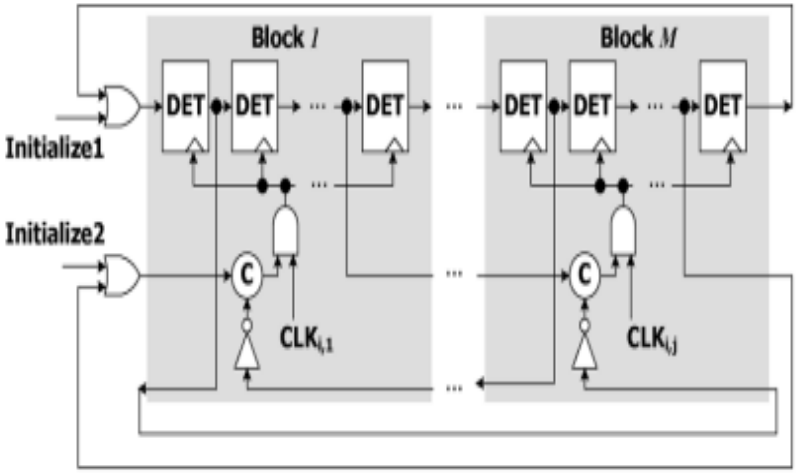

Fig 4.3: Modified Ring Counter

DET (Double edge triggered flip-flops:

Double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half The logic construction of a double-edge-triggered (DET) flip-flop, which can receive input signal at two levels the clock, is analyzed and a new circuit design of CMOS DET In this paper, we propose to use double-edge-triggered (DET) flip-flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. Double edge-

triggered flipflops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. The paper by Hossain etal[1] showed that while a single-edge triggered flipflop can be implemented by two transparent latches in series, a double edge-triggered flipflop can be implemented by two transparent latches in parallel; the circuit in Fig. 1 was given for the static flipflop implementation. The clock signal is assumed to be inverted locally. In high noise or low-voltage environments, Hossain et al noted that the p-type pass-transistors may be replaced by n-types or that all pass-transistors may be replaced by transmission gates

4.3 C ELEMENT:

The Muller **C-element**, or Muller C-gate, is a commonly used asynchronous logic component originally designed by David E. Muller. It applies logical operations on the inputs and has hysteresis. The output of the C-element reflects the inputs when the states of all inputs match. The output then remains in this state until the inputs all transition to the other state. This model can be extended to the Asymmetric C-element where some inputs only effect the operation in one of the transitions (positive or negative). The figure shows the gate-level and transistor-level implementations and symbol of the C-element.

Here is the truth table for a 2-input c-gate. Y_{n-1} denotes a "no change" condition.

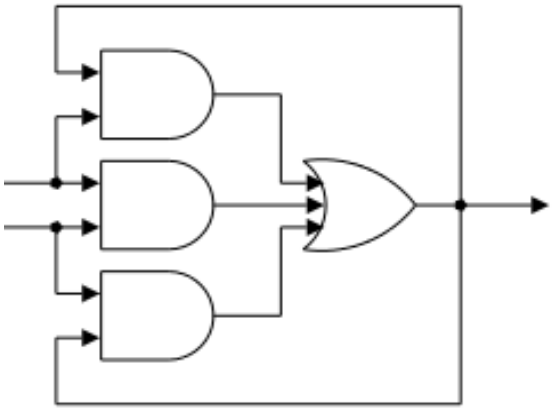

Fig 4.4: C- Element

A	B	Q
0	0	0
0	1	Q(t-1)
1	0	Q(t-1)
1	1	1

Table 3.1: Truth Table For C-Element

5. RESULT:

ISSN PRINT 2319 1775 Online 2320 7876
 Journal Volume 10, Iss 11, 2021

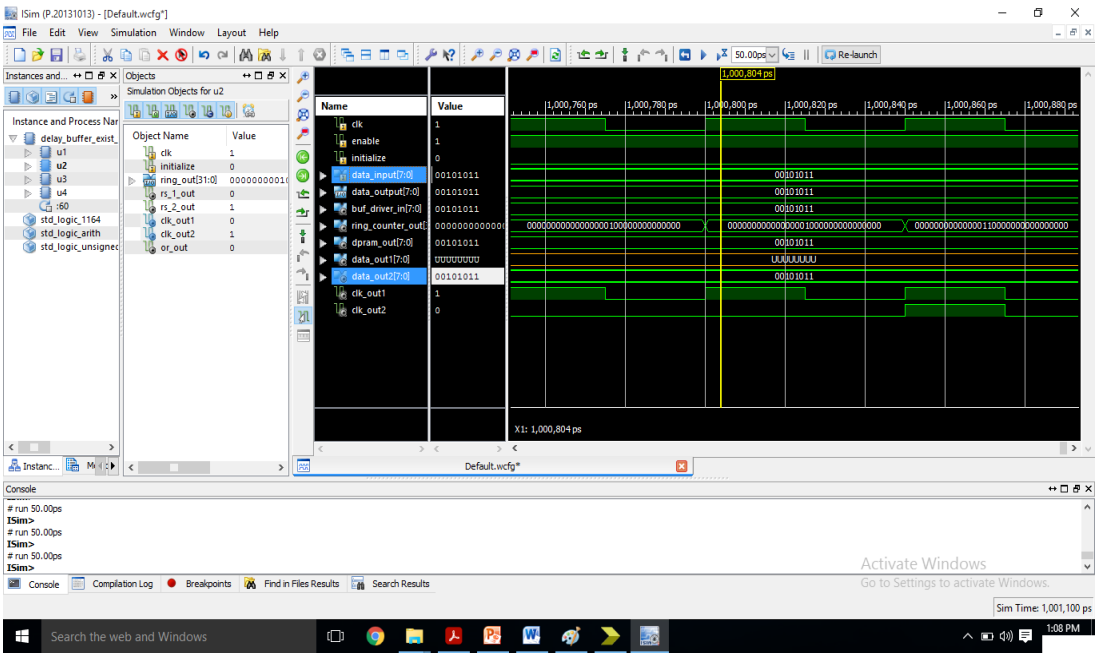

Fig: 5.1. Existing simulation output

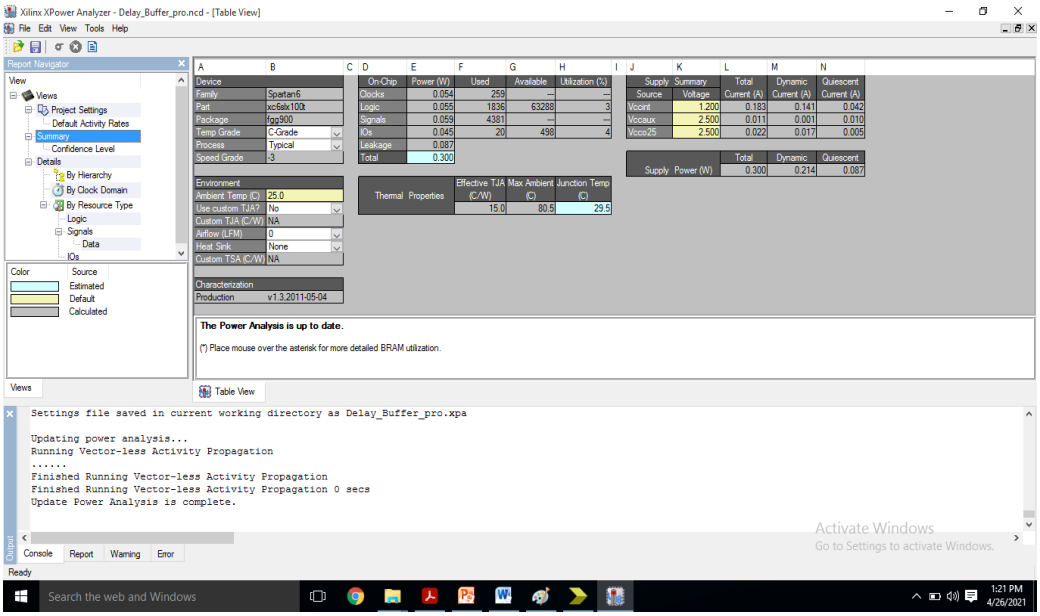

Fig:5.2.Existing power report

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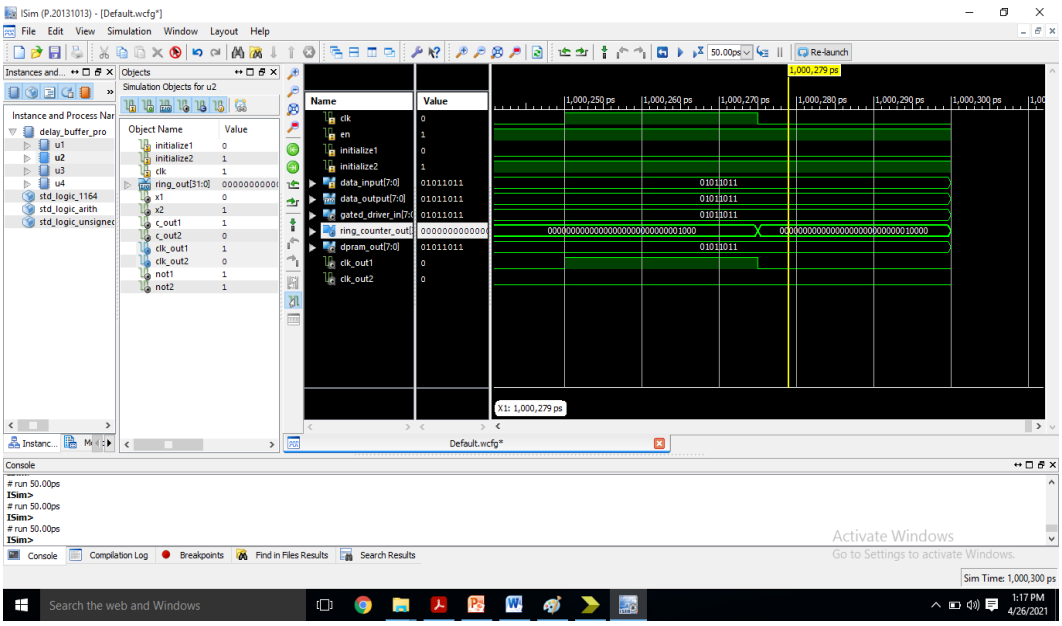

Fig:5.3. Proposed simulation output

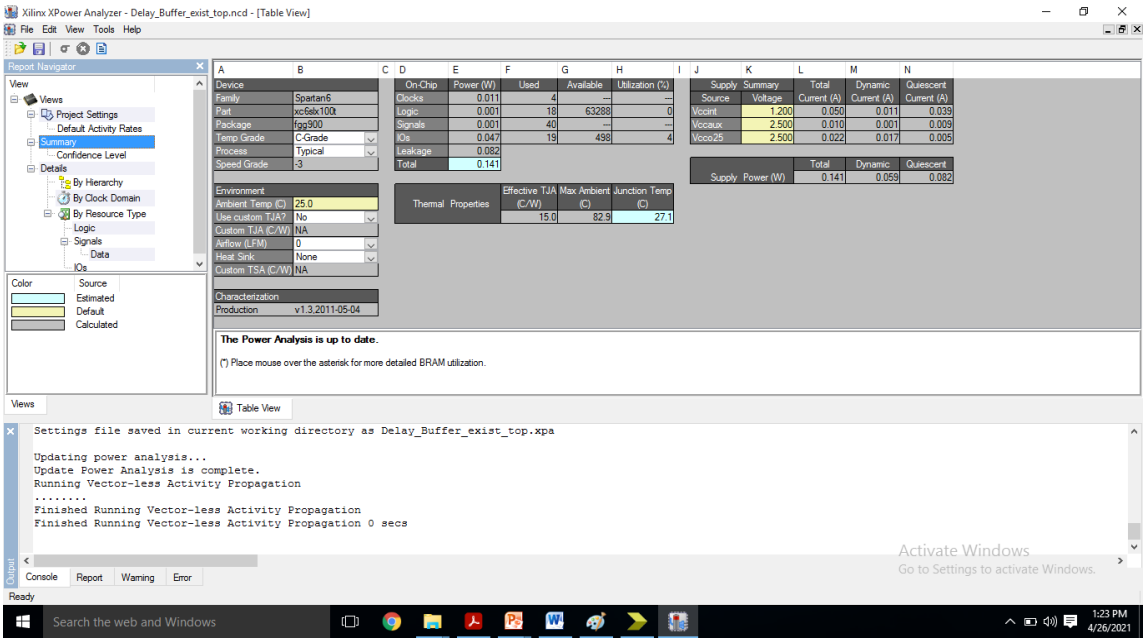

Fig:5.4. Proposed power report

ADVANTAGES:

1. Easy to use.
2. Clock source is from crystal oscillator.
3. Only need decupling capacitor. No extra component is needed.
4. No static current.

APPLICATIONS:

1. Portable memory devices like pen drives, memory cards

2. Printers
3. Washing machines, peripheral devices

6. CONCLUSION:

In this project, we presented a low-power delay buffer architecture which adopts several novel techniques to reduce power consumption. The ring counter with clock gated by the C-elements can effectively eliminate the excessive data transition without increasing loading on the global clock signal. The gated-driver tree technique used for the clock distribution networks can eliminate the power wasted on drivers that need not be activated. Another gated-de multiplexer tree and a gated-multiplexer tree are used for the input and output driving circuitry to decrease the loading of the input and output data bus. All gating signals are easily generated by a C-element taking inputs from some DET flip-flop outputs of the ring counter. We believe that with more experienced layout techniques the cell size of the proposed delay buffer can be further reduced, making it very useful in all kinds of multimedia/communication signal processing ICs.

FUTURE SCOPE:

This research work can be further extended in the following directions: reduction in vector dimension, clustering genome data, matching calculation strategy and web document clustering. Reduction in Vector Dimension - In order to improve the effectiveness of clustering further, the vector dimensionality of the data may be reduced. Clustering Genome Data - In case of genome products for exploring data from various genome databases, such as protein database, nucleic acid database and sequence database, these algorithms may be modified and applied.

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ISSN PRINT 2319 1775 Online 2320 7876
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