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MODIFIED DVSI CONTROL SCHEME FOR MICRO GRID WITH IMPROVED POWER QUALITY

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Abstract

In this project, a dual voltage source inverter (DVSI) design is proposed to enhance the reliability and power quality of the microgrid system. The devised plan incorporates two inverters, facilitating power exchange from distributed energy resources (DERs) and compensating for local nonlinear and unbalanced loads. The control algorithms are developed based on direct symmetrical component theory (DSCT) to enable DVSI operation in grid-sharing and grid-embedding modes. The suggested scheme offers increased stability, reduced bandwidth requirements for the primary inverter, lowered costs due to a decrease in the filter size, and improved utilization of microgrid control with a reduced dc-interface voltage rating for the main inverter. These features position the DVSI design as a promising alternative for microgrid applications, particularly those serving sensitive loads. The proposed topology and control strategy are validated through extensive simulation and experimental results.

I. INTRODUCTION

Innovative advance and ecological concerns drive the power framework to an outlook change with more renewable vitality sources incorporated to the system by method for appropriated era (DG). These DG units with made control out of close-by era and storerooms outline a smaller scale lattice [1]. A lattice intuitive inverter assumes a vital part in trading power from the miniaturized scale framework to the network and the associated stack [2], [3]. This small scale framework inverter can either work in a lattice sharing mode while providing a bit of neighborhood load or in matrix infusing mode, by infusing energy to the key network.

The essential focus of this work is to recognize twofold functionalities in an inverter that would give the dynamic power infusion from a sun based PV structure besides acts as a dynamic power channel, remunerating unbalances and the receptive power vital for different burdens associated with the framework.

A dispersion static compensator (DSTATCOM) is utilized for voltage heading besides for dynamic power infusion. The control plot keeps up the power adjust at the lattice terminal amid the wind varieties utilizing sliding mode control.This venture displays a double voltage source inverter (DVSI) scheme, in which the power made by the smaller scale lattice is imbued as genuine power by the fundamental voltage source inverter (MVSI) and the consonant, receptive and unequal load remuneration is performed by assistant voltage source inverter (AVSI). This has slack that the evaluated limit of MVSI can basically be used to implant genuine energy to the lattice, if satisfactory renewable power is available at the dc interface. In the DVSI plot, as total load power is given by two inverters, control misfortunes over the semiconductor switches of each inverter are decreased. This fabricates its unflinching quality when diverged from a lone inverter with multifunctional limits [13]. In like manner, more diminutive size measured inverters can work at high trading frequencies with a reduced size of interfacing inductor, the channel cost gets diminished [14]. Also, as the principle inverter is giving genuine power, theinverter needs to track the significant positive progression of current. This lessens the data transmission essential of the primary inverter.

The inverters in the proposed contrive use two separate dc joins. Since the helper

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inverter is giving zero grouping of load current, a three-organize three-leg inverter topology with a singular dc stockpiling capacitor can be used for the principle inverter. This subsequently diminishes the dc-interface voltage need of the fundamental inverter. Subsequently, the use of two separate inverters in the proposed DVSI contrive gives extended reliability, better utilization of small scale matrix control, reduced dc framework voltage rating, less data transfer capacity essential of the primary inverter, and decreased channel appraise [13]. Control calculations are created by quick symmetrical part hypothesis (ISCT) to work DVSI in network related mode, while considering non firm lattice voltage [15], [16]. The extraction of essential positive arrangement of PCC voltage is done by dq0 change [17]. The control strategy is attempted with two parallel inverters connected with a three-stage four-wire dissemination framework. Ampleness of the proposed control calculation is affirmed through organized recreation and exploratory results.

II. DUAL VOLTAGE SOURCE INVERTER

A. System Topology

The anticipated DVSI topology is showed up in Fig. 1. It involves a nuetral point cut (NPC) inverter to acknowledge AVSI and a three-leg inverter for MVSI [18]. These are connected with network at the PCC and giving a nonlinear and unbalanced load. The limit of the AVSI is to reimburse the music, receptive and unbalance fragments in load streams. Here, load streams in three stages are spoken to by i_{la}, i_{lb}, and i_{lc}, individually. Additionally, $i_{g(abc)}$, $i_{\mu gm(abc)}$, and $i_{\mu gx(abc)}$show framework streams, MVSI ebbs and flows, and AVSI ebbs and flows in three stages, independently. The dc connection of the AVSI utilizes a split capacitor topology, with two capacitors C1 and C2. The MVSI passes on the open power at appropriated vitality asset (DER) to lattice. The DER can be a dc source or an air conditioner source with rectifier coupled to dc connects. Ordinarily, renewable vitality sources like energy component and PV make control at variable low dc voltage, while the variable speed wind turbines deliver control at variable air conditioning voltage. In this way, the power created from these sources use a power shaping stage before it is connected with the commitment of MVSI. In this study, DER is being addressed as a dc source. An inductor channel is used to evacuate the high-recurrence exchanging segments created due to the trading of force electronic switches in the inverters [19]. The framework considered in this study is relied upon to have some measure of feeder resistance Rg and inductance Lg. Because of the nearness of this feeder impedance, PCC voltage is influenced with harmonics [20].

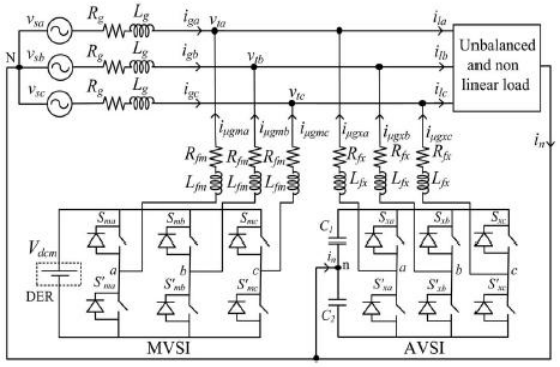

Fig. 1. Topology of proposed DVSI scheme.

B. Design of DVSI Parameters

1) AVSI: The important parameters of AVSI like dc-linkvoltage (V_{dc}), dc storage capacitors (C_1 and C_2), interfacinginductance (L_{fx}), and hysteresis band ($\pm h_x$) are chosen in view of the plan strategy for split capacitor DSTATCOM topology [16]. The dc-link voltage over every capacitor is taken as 1.6 times the peak of phase voltage. The aggregate dc-link voltage reference (V_{dcref}) is found to be 1040 V.

Estimations of dc capacitors of AVSI are picked in view of the adjustment in dc-link voltage amid drifters. Let add up to load rating is *S* kVA. In the most pessimistic scenario, the heap power may shift from least to greatest, i.e., from 0 to *S* kVA. AVSI requirements to trade real power amid transient to maintain the heap power request.This exchange of real power amid the transient will bring about deviation of capacitor voltage from its reference esteem. Accept that the voltage controller takes n cycles, i.e., $_{nT}$ seconds to act, where *T* is the system era. Henceforth, most extreme energy trade by AVSI amid transient will be *nST*. This energy will be equivalent to change in the capacitor put away energy.

Hence

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$$\frac{1}{2}C_1(V_{dcr}^2 - V_{dc1}^2) = nST \qquad (1)$$

where V_{dcr} and $V_{dc1}$are the reference dc voltage and most extraordinary permissible dc voltage across over C1 in the midst of transient, individually. Here, S =5 kVA, V_{dcr}= 520 V, V_{dc1} = 0.8 *V_{dcr}or 1.2 *V_{dcr},n = 1, and T = 0.02 s. Substituting these values in (1), the dclink capacitance (C_1) is calculated to be 2000 µF. Equalcharge of capacitance is selected for C_2. The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,h_x f_{\max}}. \qquad (2)$$

Expecting a most extreme switching frequency (f_{max}) of 10 kHz and hysteresis band (h_x) as 5%of load current (0.5 A), the estimation of L_{fx} is figured to be 26 mH.

2) MVSI: The MVSI uses a three-leg inverter topology. Itsdc-link voltage is obtained as 1.15 *V_{ml}, where $V_{ml}$is the pinnacle estimation of line voltage. This is ascertained to be 648 V. Additionally, MVSI supplies an adjusted sinusoidal current at solidarity control figure. In this way, zero arrangement exchanging music will be missing in the yield

current of MVSI. This lessens the channel necessity for MVSI when contrasted with AVSI [21]. In this examination, a channel inductance (L_{fm}) of 5 mH is used.

III. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control estimation for reference current era using ISCT requires balanced sinusoidal PCC voltages. As a result of the nearness of feeder impedance, PCC voltages are contorted. In this way, the principal positive arrangement segments of the PCC voltages are extricated for the reference current era. To change over the mutilated PCC voltages to adjusted

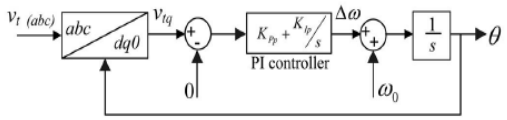

Fig. 2. Schematic diagram of PLL.

sinusoidal voltages, $dq0$ transformation is used. The PCC voltagesin natural reference frame (v_{ta}, v_{tb}, and v_{tc}) are firsttransformed into $dq0$ reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \qquad (3)$$

where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}.$$

In order to get θ, a modified synchronous reference frame (SRF)phase locked loop (PLL) is used. The schematic diagramof this PLL is shown in Fig. 2. It mainly consists of a proportionalintegral (PI) controller and an integrator. In this PLL,the SRF terminal voltage in q-axis (v_{tq}) is compared with 0 Vand the error voltage thus obtained is given to the PI controller.The frequency deviation $\Delta\omega$is then added to the reference frequency$\omega 0$ and finally given to the integrator to get θ. It can beproved that, when, $\theta = \omega 0\ t$ and by using the Park's transformationmatrix (C), q-axis voltage in $dq0$ frame becomes zero andhence the PLL will be locked to the reference frequency ($\omega 0$).As PCC voltages are distorted, the transformed voltages in $dq0$frame ($v_{td}$and v_{tq}) contain average and oscillating componentsof voltages. These can be represented as

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td}, \quad v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \qquad (4)$$

Where $\tilde{v}_{td}$ and $\tilde{v}_{tq}$ represent the average components of v_{td} and, respectively. The terms $\tilde{v}_{td}$ and$\tilde{v}_{tq}$ indicate the oscillatingcomponents of v_{td} and v_{tq} respectively. Now the fundamentalpositive sequence of PCC voltages in natural reference framecan be obtained with the help of inverse dq0 transformation asgiven by

$$\begin{bmatrix} v_{ta1}^{+} \\ v_{tb1}^{+} \\ v_{tc1}^{+} \end{bmatrix} = C^T \begin{bmatrix} \bar{v}_{td} \\ \bar{v}_{tq} \\ 0 \end{bmatrix}. \qquad (5)$$

These voltages v^{+}_{ta1}, v^{+}_{tb1}, and v^{+}_{tc1} are used in the referencecurrent generation algorithms, so as to draw balanced sinusoidalcurrents from the grid.

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B. Control Strategy of DVSI

Control strategy of DVSI is developed in such a way thatgrid and MVSI together share the active load power, and AVSIsupplies rest of the power components demanded by the load.

1. Reference Current Generation for Auxiliary Inverter: The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as P_{loss} should also be supplied by the grid. An expression for P_{loss} is determined on the condition that normal dc capacitor current is zero to keep up a steady capacitor voltage [15]. The deviation of normal capacitor current from zero will reflect as an adjustment in capacitor voltage from a relentless state esteem. A PI controller is used to generate P_{loss} term as given by

$$P_{\text{loss}} = K_{Pv}\, e_{v\text{dc}} + K_{Iv} \int e_{v\text{dc}} dt \qquad \textbf{(6)}$$

where $e_{vdc} = V_{dcref} - v_{dc}$, v_{dc} represents the actual voltagesensed and updated once in a cycle. In the above equation, $K_{Pv}$and K_{Iv}represent the proportional and integral gains of dc-linkPI controller, respectively. The P_{loss}term in this manner acquired ought to be provided by the framework, and in this manner AVSI reference streams can be gotten as given in (14). Here, the dc-connect voltage PI controller increases are chosen in order to guarantee security and better element reaction amid load change

$$\begin{aligned}
i^*_{\mu gxa} &= i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\
i^*_{\mu gxb} &= i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\
i^*_{\mu gxc} &= i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}).
\end{aligned} \qquad (7)$$

2. Reference Current Generation for Main Inverter: The MVSI supplies adjusted sinusoidal streams in view of the accessible renewable power at DER. On the off chance that MVSI misfortunes are dismissed, the influence infused to framework will be equivalent to that accessible at DER ($P_{\mu g}$). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c)

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) P_{\mu g} \qquad \textbf{(8)}$$

where $P_{\mu g}$is the available power at the dc link of MVSI.

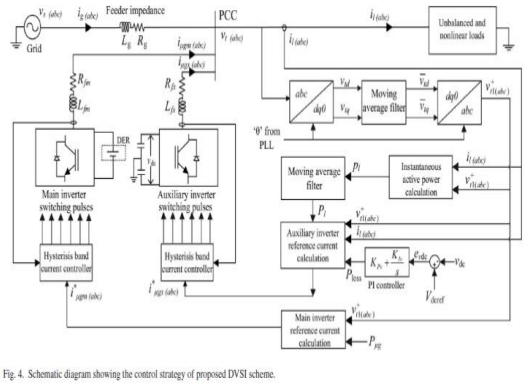

Fig. 4. Schematic diagram showing the control strategy of proposed DVSI scheme.

Fig. 3. Schematic diagram showing the control strategy of proposed DVSI scheme.

The reference streams acquired from (14) to (15) are followed by utilizing hysteresis band current controller (HBCC). HBCC plans depend on an input circle, as a rule with a two-level comparator. This controller has the benefit of pinnacle current restricting limit, great element reaction, and effortlessness in usage [14]. A hysteresis controller is a high-increase relative controller. This controller includes certain stage slack in the operation in view of the hysteresis band and won't make the framework unsteady. Additionally, the proposed DVSI plot utilizes a first-arrange inductor channel which holds the shut circle framework dependability. The whole control technique is schematically spoken to in Fig. 4. Applying Kirchoff's present law (KCL) at the PCC in Fig. 4

$$i_{\mu gx\,j} = i_{l\,j} - \left(i_{g\,j} + i_{\mu gm\,j}\right), \quad \text{for } j = a, b, c. \qquad \textbf{(9)}$$

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By using (14) and (16), an expression for reference grid currentin phase-*a* (i^*_{ga}) can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)[(P_l + P_{\text{loss}}) - P_{\mu g}]. \quad \textbf{(10)}$$

It can be observed that, if the quantity ($P_l + P_{\text{loss}}$) is greaterthan $P_{\mu g}$, the term[($P_l + P_{\text{loss}}$) $-P_{\mu g}$] will be a positive quantity,and i^*_{ga}will be in phase with v^+_{ta1}. This operation can becalled as the matrix supporting or network sharing mode, as the aggregate load control request is shared between the principle inverter and the lattice. The term,$P_{\text{loss}}$is usually very small compared to *Pl*.On the other hand, if ($P_l + P_{\text{loss}}$) is less than $P_{\mu g}$, then [(P_l+ P_{loss}) $-P_{\mu g}$] will be a negative quantity, and hence i^*_{ga}will bein phase opposition with v^+_{ta1}. This method of operation is known as the framework infusing mode, as the abundance power is infused to network.

IV.SIMULATION RESULTS

The recreation model of DVSI plan appeared in Fig. 1 is created in PSCAD 4.2.1 to assess the execution. The reenactment parameters of the framework are given in Table I. The reproduction concentrate on shows the network sharing and lattice infusing methods of operation of DVSI plan in relentless state and additionally in transient conditions.

TABLE I
System Parameters For Simulation Study

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 μF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	Z_{la} = 35 + *j*19 Ω Z_{lb} = 30 + *j*15 Ω Z_{lc} = 23 + *j*12 Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

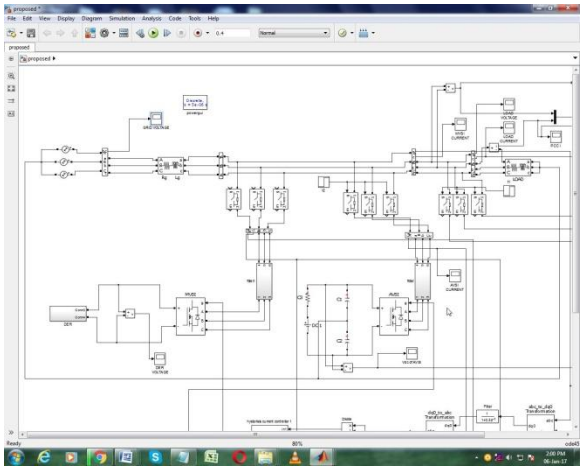

Fig.4:Block diagram

Fig.5:DER Voltage

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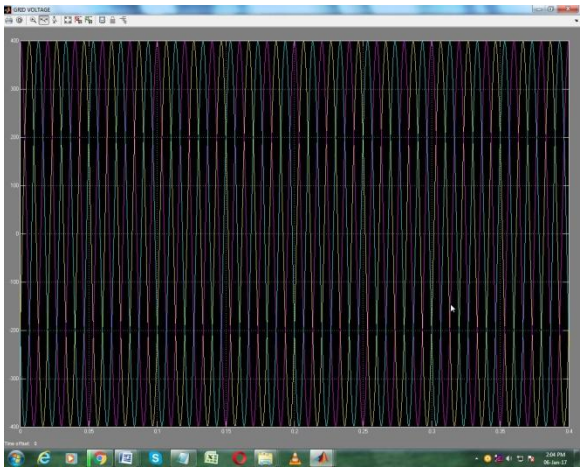

Fig.6:Grid Voltage

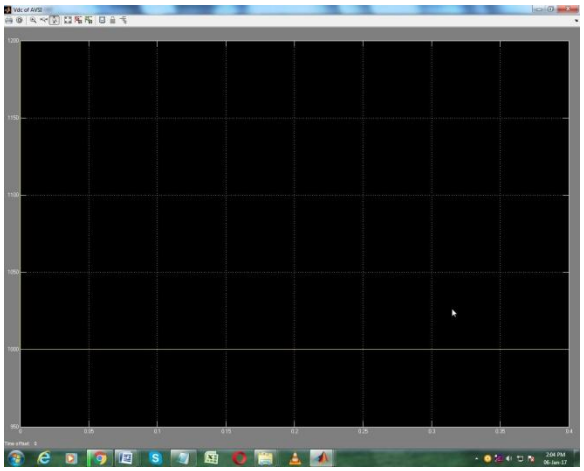

Fig.9:AVSI Voltage

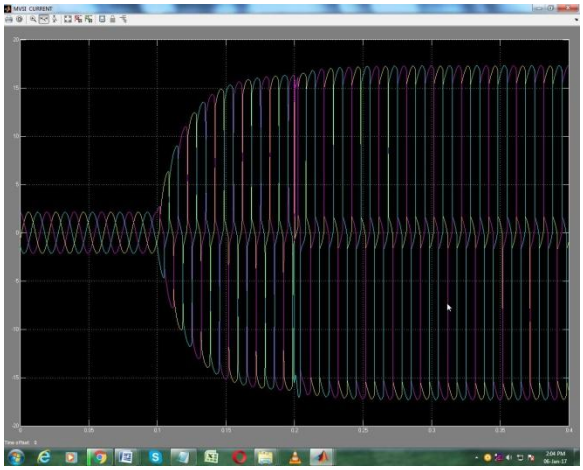

Fig.7:MVSI current

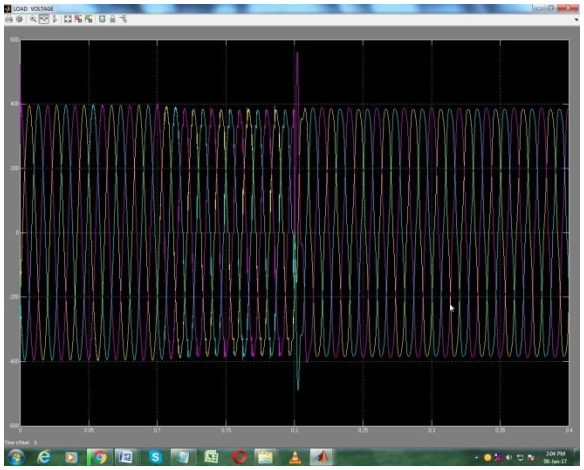

Fig.10:Load voltage

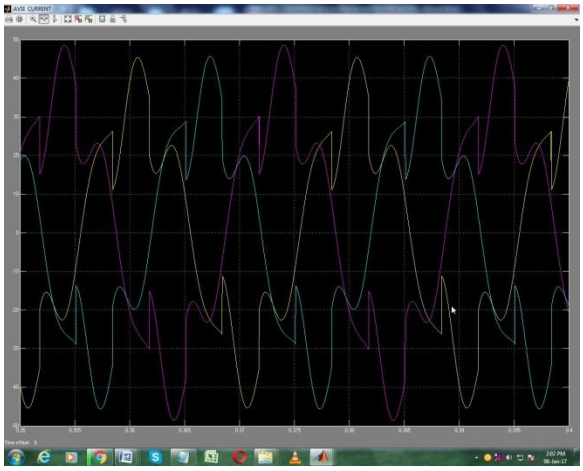

Fig.8:AVSI Current

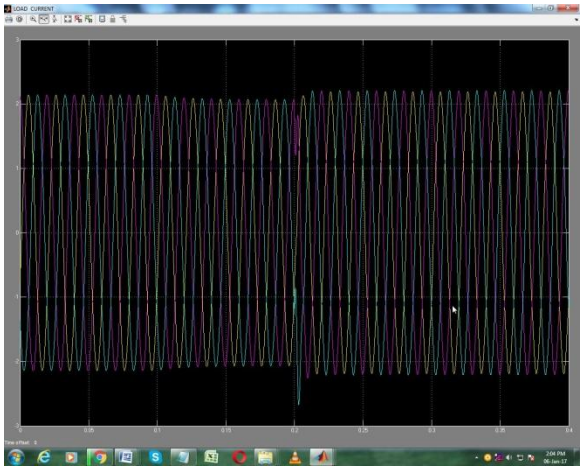

Fig.11:Load current

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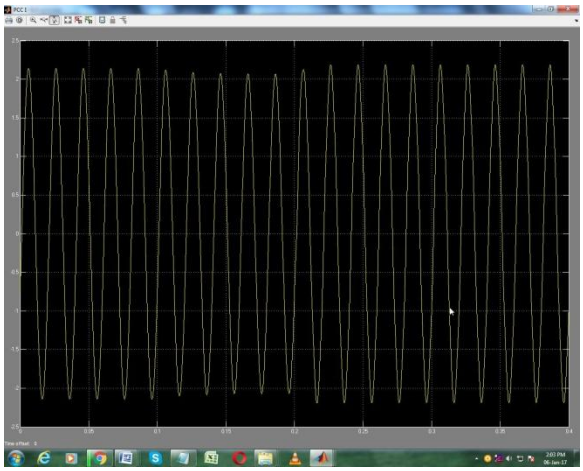

Fig.12:PCC I

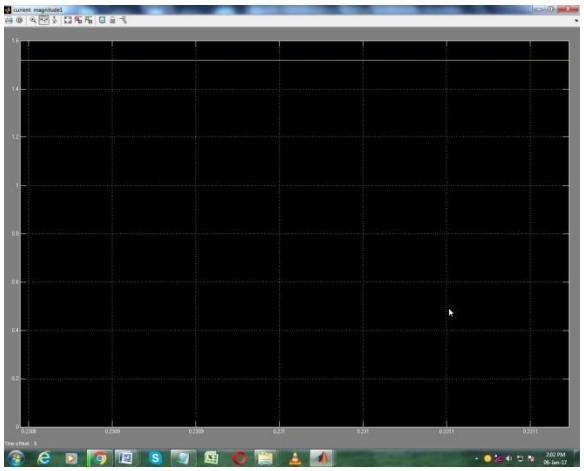

Fig.15:Current magnitude

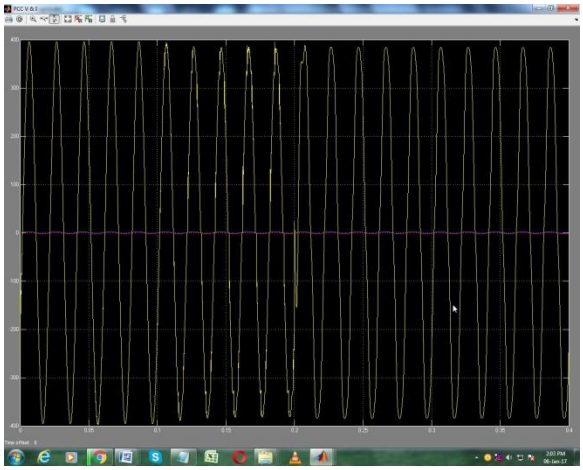

Fig.13:PCC V& I

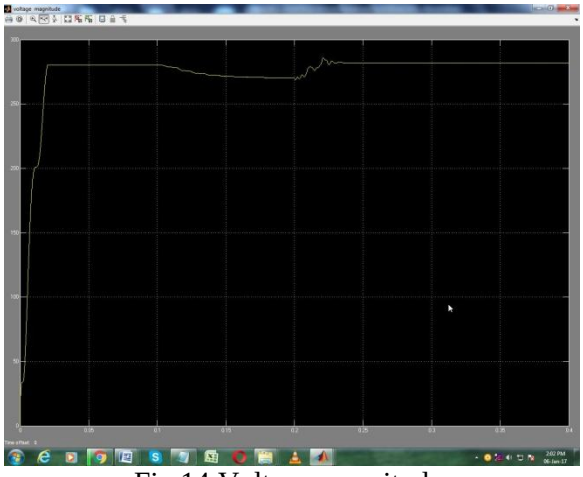

Fig.14:Voltage magnitude

V. CONCLUSION

A DVSI plan is proposed for microgrid frameworks with upgraded control quality. Control calculations are produced to create reference streams for DVSI utilizing ISCT. The proposed conspire has the capacity to trade control from dispersed generators (DGs) furthermore to repay the nearby unequal and nonlinear load. The execution of the proposed conspire has been approved through reproduction and exploratory studies. When contrasted with a solitary inverter with multifunctional abilities, a DVSI has numerous preferences, for example, expanded dependability, bring down cost because of the diminishment in channel size, and more usage of inverter ability to infuse genuine power from DGs to microgrid. Also, the utilization of three-stage, threewire topology for the primary inverter lessens the dc-connect voltage prerequisite. Along these lines, a DVSI plan is an appropriate interfacing choice for microgrid providing delicate burdens.

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