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MULTILEVEL BOOST INVERTER WITH SWITCHED CAPACITOR FOR SMART GRID APPLICATIONS

[1]**Pagidela Yamuna**, Assistant Professor (Adhoc), Department of EEE, JNTUACEP, yamuna.pagidela@gmail.com
[2]**K.Ravisankar**, Assistant Professor (Adhoc), Department of EEE,JNTUACEP,krs.sai@gmail.com
[3]**P.Janaki**, 1Assoc. Prof., Department of EEE, Lendi Institute of Engineering & Technology, janaki.pakalapati@gmail.com
[4]**N.Madhava Reddy**, Assistant Professor (Adhoc), Department of CIVIL, JNTUACEP, nmmadhava136.ce@jntua.ac.in
[5]**Vempalle Rafi,** Assistant Professor (Adhoc), Department of EEE,JNTUACEP, vempallerafi@gmail.com

Abstract. Power electronic Inverters that are required to connect Direct Current power sources to the Alternating Current grid. Conventional inverters frequently employ massive, costly, and lossy transformers and harmonic filters. Currently, reduced number of circuit components and voltage sources are considered as one of the most important features in Multi-Level Inverters (MLIs). These are a potential adjunct to traditional inverters, providing lower THD, an inductor-free design, and a wider range of operation. These generate a stepped waveform that closely resembles a sine waveform. Smart grids may include multiple sources, and whenever these sources have low THD, the demand for monitoring data at the site of common coupling is minimized. Two switching multilevel inverters of capacitor-based with boost capabilities and reduced THD are suggested in this study. The inverters contain built-in charge balancing, eliminating the need for voltage sensors and additional circuits. Phase Disposition PWM (PDPWM) technology is used to modulate the switches in the inverters, allowing for better voltage regulation and lower switching losses. Simulation is used to validate the designs, the parameters and output waveforms are shown.

Index Terms: Multi-Level Inverters (MLIs),Switched Capacitor, PDPWM technology, Smart Grid, THD

I INTRODUCTION

Industries have grown to require greater power equipment in recent years, even exceeding the megawatt level. Power electronics is the use of solid-state electronics to regulate and convert electrical power. These gadgets are presently the most significant component in obtaining energy from renewable sources. In high-powered applications, efficiency is critical for AC-to-DC conversion or vice versa. Power Electronics provides extremely efficient power conversion, minimising heat losses and, as a result, device size.Inverters were indeed power electronic elements which convert direct current voltages to alternating current waveforms. Based on the application, the output frequency could be constant or changing. A waveforms that closely approaches a sine wave has the lowest possible harmonic distortion, and it rises as the voltage output waveform deviates from the sine wave. When fed to an AC motor, those harmonics induce higher losses and create pulsing torques [1, 2].

Adjustable frequency drives, air conditioners, UPS, arc furnaces, hvdc power transmission, EV drives, voltage regulators, active filters, and flexible AC transmission networks all rely on these devices. They are often used to convert the direct current (DC) power widely obtained from passive components to the alternating current (AC) power required for prevalent electrical loads.Inverters are categorized into four types based on the nature of their output waveform: multilevel inverters, square wave inverters, two-level PWM inverters, and quasi-square wave inverters.

THD is a representation of the percentage of harmonics in a signal. These frequencies are multiples of the primary

frequency in integral terms. Harmonics reduction is critical since they distort the signal and cause system losses.Managing harmonics even atPCC(point of common coupling) becomes a problem in smart grids due to the existence of several dispersed sources. MLIs are a profitable power conversion alternatives since they are easy to manage and excellent for lower harmonics power injections. Passive filters have been widely accessible to minimise these harmonics. However, the primary problem to these filters would be that while the capacitor and inductor are quite big to be practical as well as economical for least significant harmonics at 50 Hz.

Power electronics enable the conversion of produced electric energy into its desired by the load. Theyalso an essential element of the system that comprises a country's power grid

Among their benefits are:

1.Reduce energy use by reducing losses

2. Improve the power system's functioning

3. Allow for the incorporation of renewable

4. Aid in the development of a low-carbon energy environment

The losses in transmission can also be minimized in the power grid by using HVDC Transmission systems wherein inverters and converters are used for efficient power conversion.

II MULTILEVELINVERTERS

The demand for extremely efficient and high-quality electricity has given rise to a new type of inverter known as multilevel converters. They consist of a series of power semiconductors and capacitor voltage sources, the output of which produces voltages with stepped waveforms.Multilevel converters are a type of inverter that generates a waveform with a stepped pattern similar to a sine waveform. These are often better prevalent since they do not necessitate the use of transformers and inductors for energy conversion. One of the numerous possible Pulse Width Modulation methods is used to create the necessary stepped waveform.The primary goal of MLIs is to generate a wave that is as close to a pure sine wave as feasible. The reduction in total part count in comparison to traditional topologies has been a key goal in the recently proposed multilevel architectures

The three most common multilevel inverter architectures are cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitors (FCs). Cascaded MLIs provide dependable performance and can achieve greater output voltage [4].All such inverters provide good quality of power even with a low number of power switches [5]. Conventional converters suffer from the need the use of several supplementary circuit devices for capacitor charge equalizationin order to achieve the required functioning [6, 7]. Because the magnitude of the output voltages not be more than the proportional overlaying of the DC connection voltages, these converters do not have an enhance function [8]. Alternate topologies for CHBs with fewer switches for the same rated power and greater THD reduction are current developments in multilevel inverters.

The limited magnitude of available DC source voltage is one of the key problems confronting the rapidly developing solar renewable energy system.Since most loads operate at higher voltage than the panel output voltage, a boost converter, which steps up DC voltages from low values to high values without the use of a transformer is often employed before converting it to alternating current (AC) via an inverter. Because of their inherent voltage boosting capabilities and the significant reduction in the voltage sources require to generate a large magnitude output waveform, capacitor-based switching systems are a viable alternative.

Multi-level inverters are a feasible and more efficient alternative to traditional inverters. These inverters feature advantages such as minimal switch stress, low harmonic distortion, and the ability to be used in both high voltage and high-powerscenarios.MLIs are utilized in both low-power and high-power operations such as UPS, induction motor drives, as well as FACTS.

II.I Base circuit configuration andworking

Figure 1 depicts the circuit presented in the base article. While functioning at a lower switching frequency, the

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inverter may provide 19 levels of output voltage. The following are the primary characteristics of switched capacitor-based circuits. Several authors have suggested MLIs with innovative switching capacitor architectures. These models prioritise dependability while minimising component prices and power dissipation.The inverter of 19-level with switched capacitors was the first to be studied and simulated.

1.The ability to boost the output voltage.
2.Generating a large number of voltage levels with only four electrolytic capacitors and two voltage sources.
3.Minimum power switches and gate drivers are used, with a low switching frequency.
4.Reduction of total switching loss through the use of the HPWM technique.
5.Self-balancing capabilities, which eliminates the requirement for extra charge balancing circuits.

Switched capacitor inverters provide numerous advantages, including excellent reliability, low cost, simple component changing, and reduced the requirement of DC sources. The primary problem is that they need precise voltage or charge balance. This may be accomplished in an open loop by allowing sufficient switching and current transit routes for natural charge balancing per cycle. It may also be implemented in a closed system or with an RLC filters set to the operating frequency and connected in parallel configuration with the load. This raises the expenses and reduces the circuit's transient responsiveness. When implemented to an optimal and balanced circuit, the PDPWM approach is said to be the optimum way to use for a MLI of capacitor-basedsince it provides self-sufficiency.

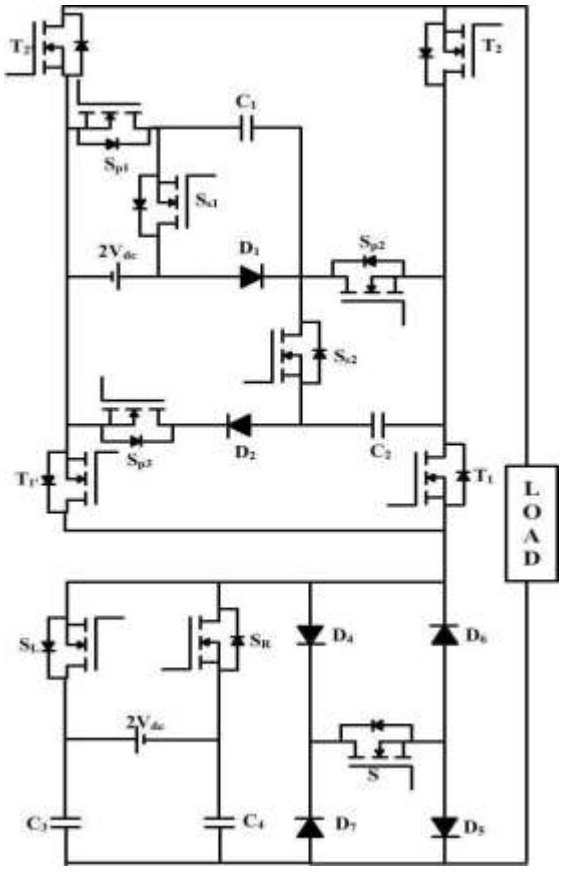

FIGURE 1 Basic circuit diagram

So the suggested hybridised structure would create a output voltage of 19-level, the adoption of 18 carrier waveform may enhance the elements intricacy. Because the HPWM method uses fundamental and higher switching

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frequencies in hybrid MLVSIs reduced the impact of switching losses. The circuit was implemented in Matlab, and the output waveform for voltage is depicted in Figure 2

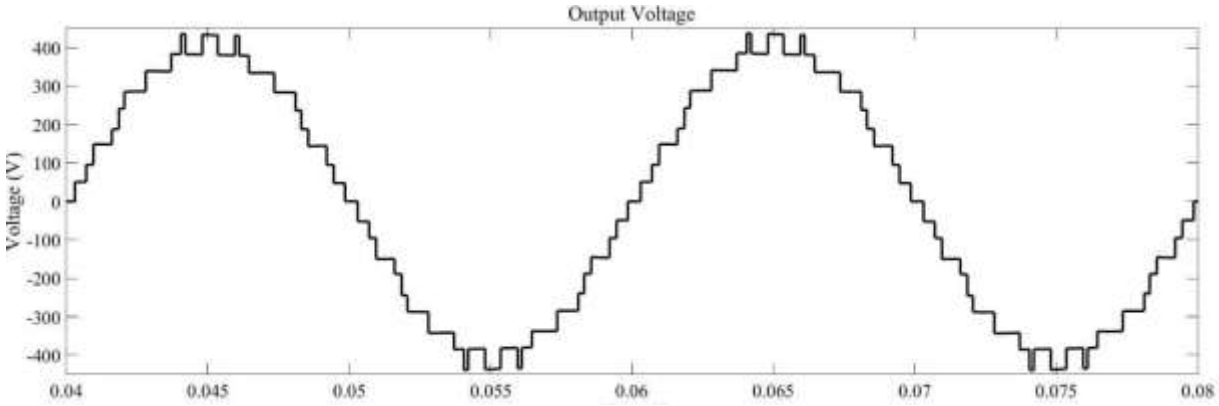

FIGURE 2. Total Output Voltage

II.II Novel Topology1

The suggested topology's power circuit, seen in Figure 3, is made up of 2 separate switched capacitorbased cells, the Floating Capacitor (FC) cell and the Switched Capacitor (SC) cell, that operate in combination to generate the required output waveform of 19-level.

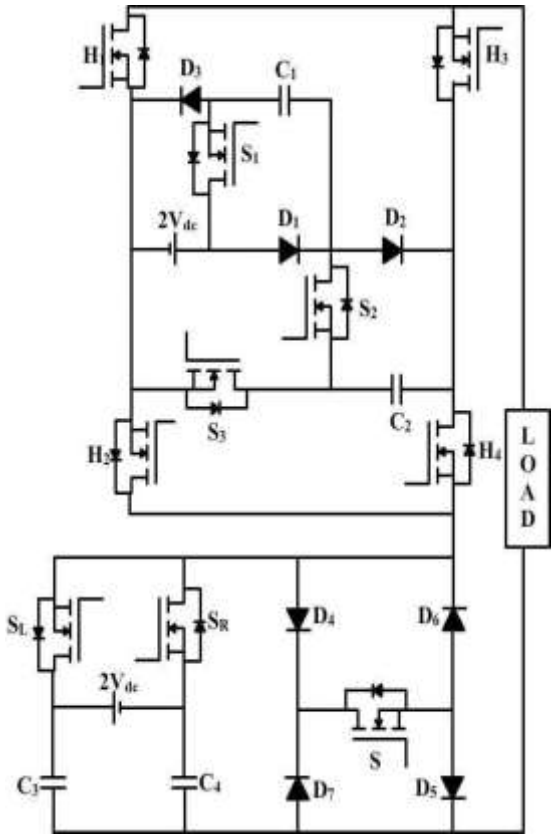

FIGURE 3. Proposed Novel Topology 1

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Each cell makes use of a one source of DCvoltage and two capacitors, which will then be switched appropriately to generate separate 3-leveland 9-level waveforms.The SC cell has a lower switching frequency, whereas the FC cell has a greater switching frequency. The SC cell generates a 9-level waveform with one zero level, four positive and four negative level. The FC cell generates a 3-level waveform with one zero level, one positive and one negative level. The inverter may generate a staggered sine wave with maximum amplitude nine times higher than the DC sourcevoltage by connecting SC and FC cells in series.

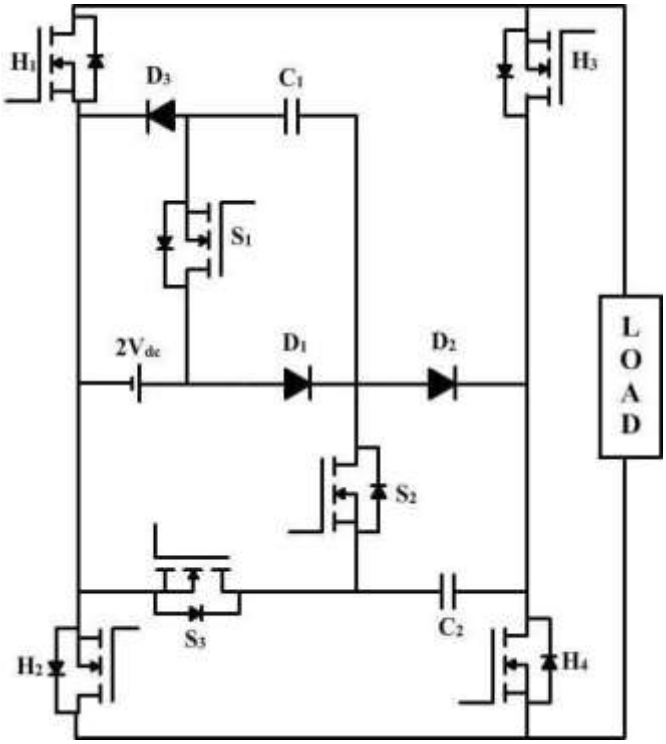

FIGURE 3.1 SC cell ofNT1

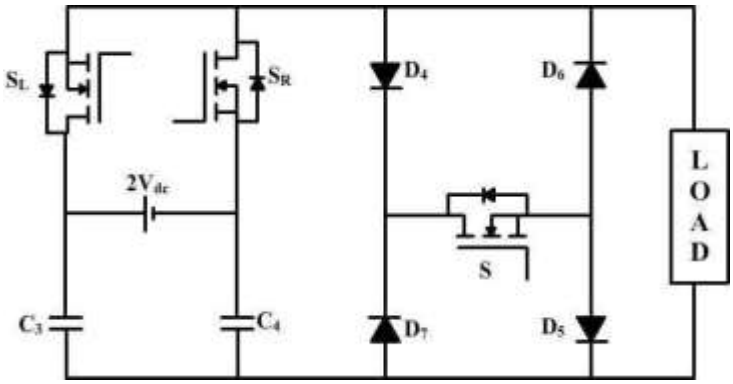

FIGURE 3.2 FC cell ofNT1

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This is accomplished by the use of 10 MOSFET switches, 3 diodes and 4 capacitors. The switched capacitor network is formed by the capacitor and diodes, and it provides voltage enhancing capabilities.Capacitor Voltage leveling of is accomplished by series to parallel flipping of the capacitor circuitry using semiconductor switches, resulting in consistent switching cycles that circuit to function with lower switching losses and a lower switching frequency the Phase Disposition PWM (PDPWM) approach is employed

II.III Novel Topology2

The converter circuit is made up of nine switches, three diodes, two capacitors, and two DC power sources. This research looks at a symmetric arrangement in which twopower supplies have almost the same amount of voltage. The two capacitors serve as memory components, and they are charged and dissipated many instances during that operation.At every step, each switch is turned on and off to produce a distinct voltage output, resulting in a multilevel voltage waveform. When this multilayer waveform is put into an H-Bridge, it generates a multilevel AC output voltage with low THD. The possibilities of each capacitor charging step may be separated into two modes:

1. Turned onS4 Switch, and turned off S5 Switch
2. Turned onS5 Switch, and turned off S4Switch

In first mode, the charging circuit has simply one voltage source. In second mode, the charging circuit contains both voltagesources. Each voltage source is considered to have a magnitude of 100V. As a result, during the operation of the circuit, capacitor C1 is charged to voltages of 100V and 200V, while capacitor C2 is charged to voltages of 200V and 400V. Thus, various output voltages are achieved at each step by series-parallel swapping of the sources voltage using the capacitors, which is assisted by power electronic devices. The suggested power circuit is depicted schematically in Fig. 4.

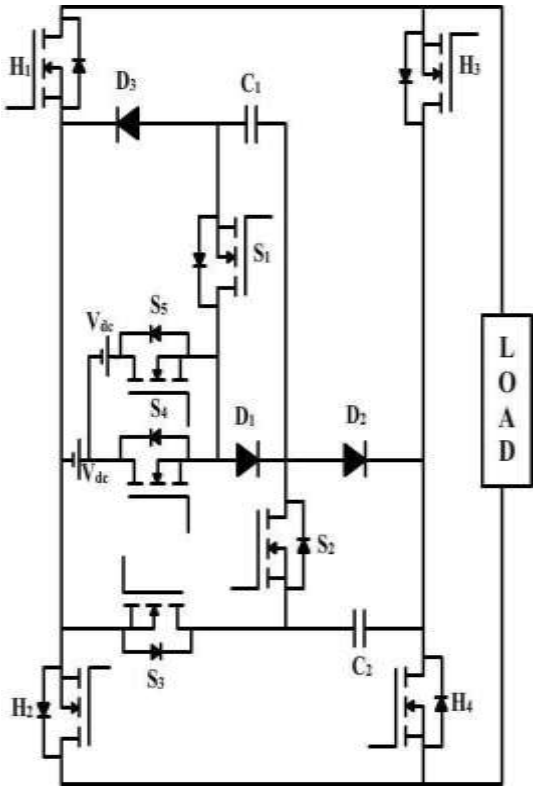

FIGURE4 Proposed Novel Topology 2

Two capacitors were self-charge balance throughout each operation, eliminating the requirement for exterior circuits to disperse the concentrations. These are accomplished by series-parallel swapping of a capacitor connection utilising PDPWM. It thusenables complicated gate inputs to turn ON and turn OFF of the switches numerous cycles over a period, resulting in storing and draining pathways and contradictions.

III PWM technique proposed

The switching signals for such switches in each of the mentioned architectures are produced by comparing a standard sine wave with carriers that closely approaches the required output voltage. The approach employed in this study is known asPDPWM(Phase Disposition PWM), and it compares the actual potential of a standard sine wave to 9 level displaced triangular waveform during in its first configuration and 8 level displaced triangular waveform in the second configuration. The amplitude of the standard sine wave is set to 9 or 8, and the amplitudes of triangular waves are set to 1.

The sine wave that is used as a reference is described as follows:

$$Vref = Ar \sin wt$$

The modulation index is obtained from the following equation:

$$m = \frac{Ar}{n * Ac}$$

Here Ac represents the each waveform amplitude, n is the quantity of triangular waveform, Ar represents the standard sine wave amplitude. In the first and second topologies, Ar is selected as 9 and 8, respectively, while Ac is set as 1. As a result, the modulation index usually estimated to be 1. In this example, this enables for the greatest amount of levels to be acquired while minimising THD. Also described is a commander coefficient (CM), which is used to choose thepositively or negatively of the standard wave throughout a single operation.

$$CM = \frac{1 + \text{sgn}(Vref)}{2}$$

where $Vref = Ar \sin(wt)$

When CM = 1, the comparative analysis between Vref and each carrier waveform is performed in the first half-cycle of the reference waveform, resulting in positive output voltage levels, whereas when CM = 0, the comparison is performed during second half-cycle of the standard waveform, resulting in negative levels of output voltage.

IV RESULTS

IV.I Simulation results of Novel Topology 1

For all topologies, the goal of this research is to reduce THD for a resistive load of 200 ohm. The THD of the output voltage and current waveforms was calculated using the FFT Analyzer.MATLAB Simulink r2018a was used to model the suggested 19-level SCMLI. For simulation, the Simscape PowerSystems toolkit was utilised. The solver Tustin/Backward Euler was used.

The suggested inverter module's outputwaveform is seen in Figure 5. The load current was subjected to FFT analysis, and the results are presented.. The load current's THD was discovered to be 5.80 percent. The output current's third harmonic component was determined to be 0.47 percent.

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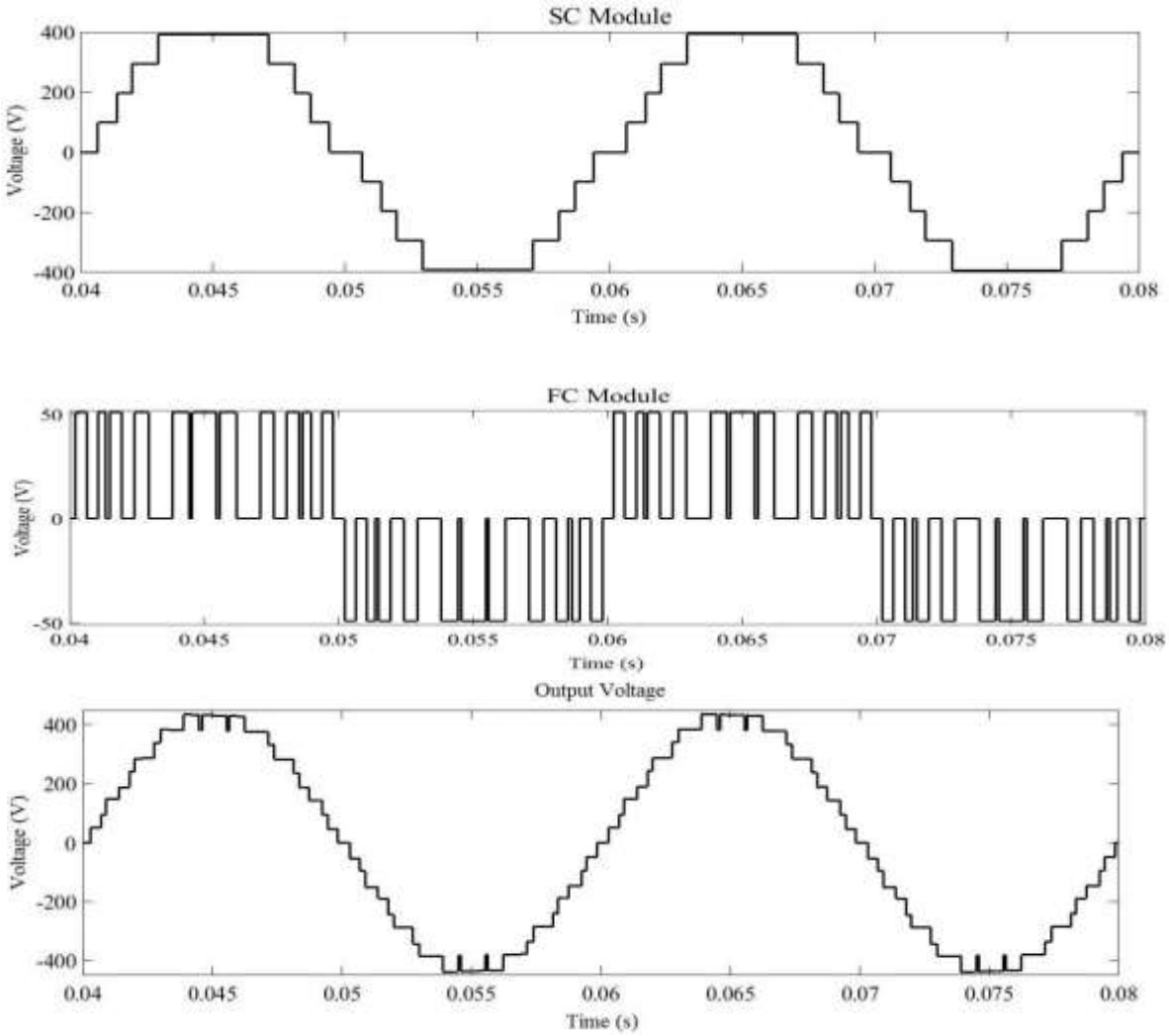

FIGURE 5. Output waveform of NT1 (a) SC Module (b) FC Module(c) Overall Output Voltage

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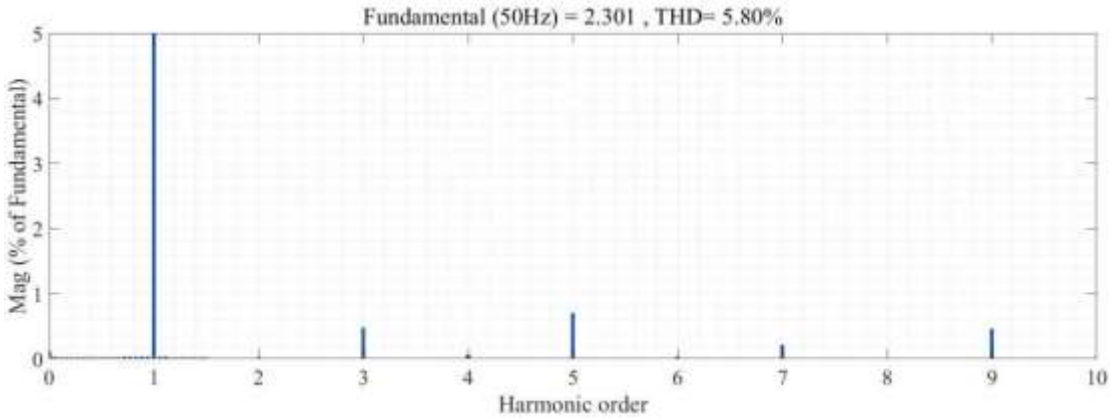

FIGURE6.THD characteristics of NT1 output current

IV.II Simulation results of Novel Topology 2

MATLAB Simulink r2018a was used to model the suggested 17-level SCMLI. For simulation, the Simscape PowerSystems toolkit was utilised. The solver Tustin/Backward Euler was used.For all topologies, the goal of this research is to reduce THD for a resistive load of 200 ohm.

The THD of the output voltage and current waveforms was calculated using the FFT Analyzer.The load current's THD was discovered to be 6.41 percent. The output current's third harmonic component was determined to be 1.71 percent.

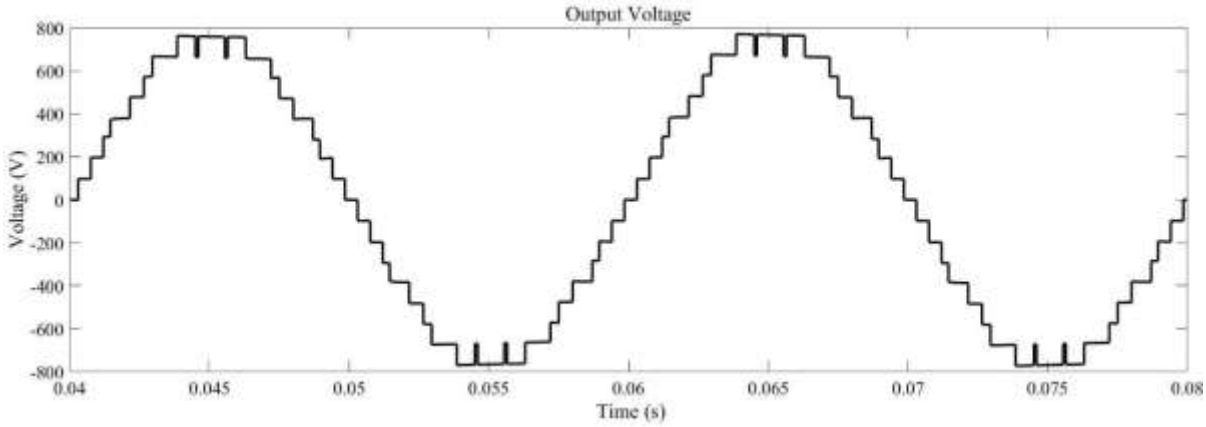

FIGURE 7 Output waveform of NT2

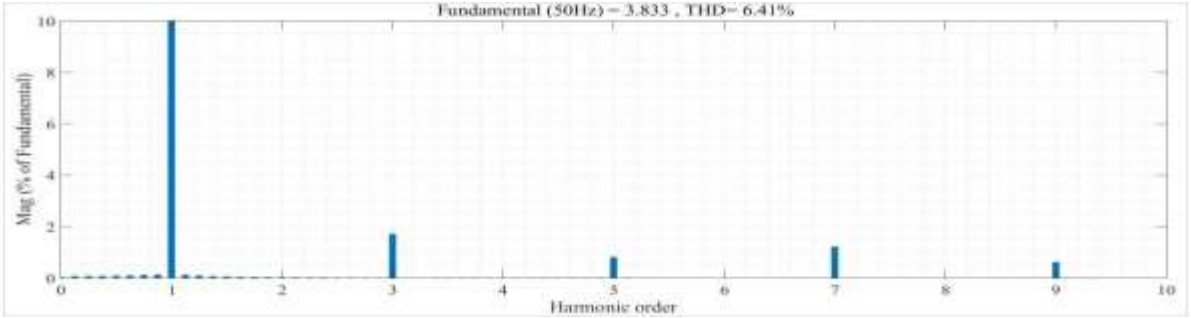

FIGURE8. NT2 output current THD characteristics

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V CONCLUSIONS

The initial step in this project is to replicate a single phase multi-level inverter based on switching capacitors using fewer components. Then, based on the simulated model, two innovative designs are presented, with the models focusing on decreasing losses and expenses with boosting dependability.The various topologies of multi-level inverters as well as novel PWM methods were discussed.Switching pulses were generated using the carrier-based PDPWM method. A resistive load's voltage and current output waveforms were recorded. The Simscape Power Systems toolkit was used to simulate in the MATLAB Simulink framework. The THD was calculated using an FFT analysis.

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