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ANALYSUIS ON CHARACTERISTIC PARAMETERS OF NANO SCALE MOSFETS AND THEIR APPLICATIONS IN LOW POWER VLSI CIRCUITS

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ABSTRACT

There is no denying the revolutionary impact that semiconductors have had on society. Although communication and data processing have likely always been essential, the advent of semiconductors has made both incredibly simple and far more efficient than they were, for example, in the era of vacuum tubes. Researchers can therefore pick an appropriate level of abstraction for their needs. Power, speed o performance, silicon area, and cost are the most critical factors in VLSI architectures. Some systems are based on extremely low power operations, while others are performance efficient. There has been a lot of study, but most of it has been at the circuit level. Many different logic architectures and methods for lowering power consumption in circuits have been mentioned in the literature as potential means of accomplishing this goal. As a result, very few methods for achieving that low power design target are provided. In recent years, low power VLSI design has been increasingly interested in sub-threshold logics. The dynamic and leaky power in the super-threshold region can also be decreased by adopting an adiabatic logic style. To account for these factors in complicated circuits, I have provided an analytical model of power dissipation and propagation delay in a subthreshold inverter.

1. INTRODUCTION

From Michael Faraday in 1833 through the first silicon transistor in 1954, which ushered in the era of silicon electronics and microelectronics [1]-[11], the history of semiconductor material research is charted. Band theory has helped unify previously disjointed and technology-driven efforts. An burst of activity in semiconductor studies, which has persisted to the present day, occurred, however, with the development of this successful quantum theory of solids, as well as a focus on the growth of pure silicon and germanium and an understanding of their properties.

A semiconductor amplifier based on the field effect principal was first proposed by William Shockley in 1945. The notion stemmed from the observation that a transverse electric field can alter the conductance of a semiconductor layer. Unfortunately, at the time, experimental confirmation of the concept was not possible. John Bardeen began developing the field effect device in 1947 after publishing a surface theory in support of the concept. Power gain from a germanium point-contact transistor device was first shown by John Bardeen and Walter Brattain in December 1947. However, questions remained unanswered about how the transistor worked. Shockley's discovery of minority carrier conduction led Bardeen and Brattain to conclude that surface-related events played a crucial part in the field effect device. Schookley conceptualised the p-n junction and junction transistor within a month.

Gordon K. Teal and John B. Little, working off the Czochralski method, created the

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technology that Bardeen and Brattain used to prepare the semiconductor material they worked with. The crystal was then refined utilising William G. Pfann's zone refining technique. Early transistors had point contacts, which made them unstable and made it difficult to regulate their electrical characteristics. It wasn't until 1952 that the first grown junction transistors entered production. Devices similar to modern MESFETs and MOSFETs were patented by Julius Lilienfeld in 1930 and 1933. Capacitive control in field-effect transistors was the subject of a patent application by Oskar Heil in 1934. Because the semiconductor surface wasn't adequately passivated, early bipolar transistors were notoriously unstable. M. M. Atalla led a team that investigated this issue and determined that a silicon dioxide coating might help. In the course of this research, a novel field-effect transistor design was conceived of and then realised in physical form. The device's inability to compete with bipolar transistors' performance led to its eventual oblivion. Paul Weimer and TorkelWallmark of RCA worked on a similar device to the MOS transistor years before Bell Laboratories presented one.

2. LTERATURE REVIEW

2.1 INTRODUCTION

A thorough understanding of the major variables, ideas, and phenomena, as well as the methodologies and history of a subject of study, is demonstrated through a literature review, which is therefore of great importance in the realm of research. The student can learn more about the leading scholars and research institutions in the topic by conducting a literature review. There are several scientific reasons for performing a literature review beyond the aforementioned reasons for writing a review (i.e., proof of knowledge, a publishable document, and the identification of a research family).

1. a distinct understanding of what has been completed and what remains to be done.

2. Identification of the most important factors that bear on the subject at hand

3. putting things together and seeing things differently

finding connections between theories and methods (point 4)

5. realising the relevance of the issue and providing an explanation; 6. connecting abstract concepts with practical situations 7. naming the primary approaches and methods that have been employed

Therefore, in this section, we provide a comprehensive literature evaluation of the planned study. As the market for implanted biomedical systems (such as hearing aids) and other portable devices (such as smart phones, smart watches, etc.) continues to grow, the necessity for creating low power logic circuits has become critical. In such gadgets, power consumption is more important than processing performance. Because the threshold voltage was higher in the past, switching energy has been prioritised over leakage energy. Since dynamic or switching energy is directly proportional to the square of the supply voltage, lowering the supply voltage has a major impact on lowering switching energy consumption. Energy required to switch also depends on factors such as the frequency of switching, the capacitance of the output node, and so on. There have been several reports of circuit-level strategies for lowering switching energy. Adiabatic logic is a potentially game-changing method for drastically cutting down on wasted energy while switching. However, high performance operations cannot make use of adiabatic logic types. Circuit-level design approaches exist for

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minimising super-threshold regime static and dynamic power consumption.

2.1.1 Sub-threshold Slope:

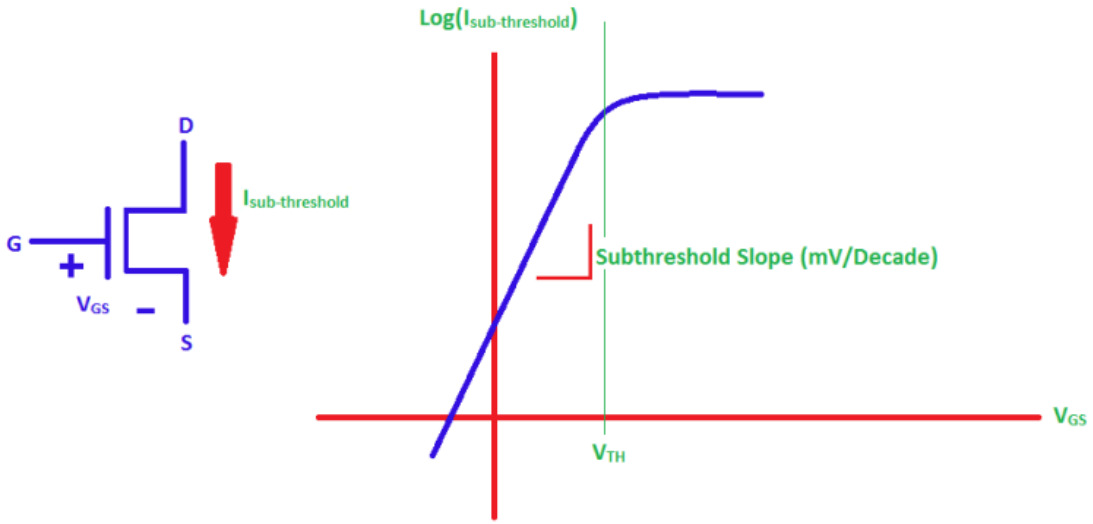

Fig. 2.1 Sub-threshold slope of MOSFET

As shown in Fig. 2, the most crucial metric for gauging the switching of the device is the sub-threshold slope, which is connected to the MOSFET's V-I characteristics.1. For a given drain-to-source current IDS and gate-to-source voltage VGS, the Subthreshold swing (S) is calculated as S = (d log IDS/dVGS) 1. The swing below the sub-threshold has a significant effect on the leakage power. The sub-threshold swing specifies the smallest value of VGS reduction that yields a tenfold improvement in sub-VT regime IDS. The higher the Sub-threshold slope, the smaller the Sub-threshold swing. Nanowire field-effect transistors (NWFETs) [4, 6], carbon nano tube-based tunnel field-effect transistors (T-CNFETs) [6, 7], and impactionization MOS-based transistors (IMOSs) [5, 6] all have S values (sub-kT/q) that are lower than those of Bulk, FinFET, and fully-depleted silicon-on-insulator (FDSOI) MOSFETs at room temperature. Among these high-switching devices, a TFET stands out due to its low OFF current [8]- [22] and compatibility with the CMOS technology.

3. POWER DELAY MODELING OF CMOS CIRCUITS IN SUB-THRESHOLD REGIME

3.1. INTRODUCTION

Due to the proliferation of mobile communication and sensing devices, ultra-low power design has become increasingly important in recent years[1, 2]. However, low-power applications don't always require peak performance. In mobile wireless applications, sensor nodes, body implanted devices, etc., low power dissipation is more important than performance. When operating at sub-threshold voltages, CMOS logic circuits [3]-[5] achieve ultralow power dissipation at the expense of relative slowness. In order to further enhance ultra-low power logic circuits in the sub-threshold zone, an in-depth investigation of power dissipation is required.

Numerous papers [1–7] have examined DC behaviour in sub-threshold logic circuits. These studies [3, 5]-[8] have focused less on power dissipations and more on the latency and noise margin of logic circuits. To date, the

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majority of studies devoted to analysing power dissipation have relied on oversimplified models [9, 12]. Here, the same design method utilised by super-threshold logic circuits is applied to express the power dissipation of a sub-threshold logic inverter. Power dissipation is sometimes oversimplified as Pdiss=fCLVDD 2, however this ignores the crucial contributions of the device characteristics, most notably static leakage, which is a problem in the sub-threshold region. [11]. To improve the accuracy of the suggested model for nano-scale MOSFET devices, short channel effects must be accounted for. On the basis of the manufactured chips, only a few analyses have been conducted, all of which have failed to analytically explain the power dissipation [9, 13], [14].

3.2. BEHAVIOR OF MOSFET IN SUB-THRESHOLD REGIME

For NMOSs, we can write the sub-threshold drain-source leakage current [13] as,

$$I = I_0\left(\frac{W}{L}\right)e^{\frac{V_{GS}-V_{TH}}{mV_t}}\left(1-e^{-V_{DS}/V_t}\right)$$

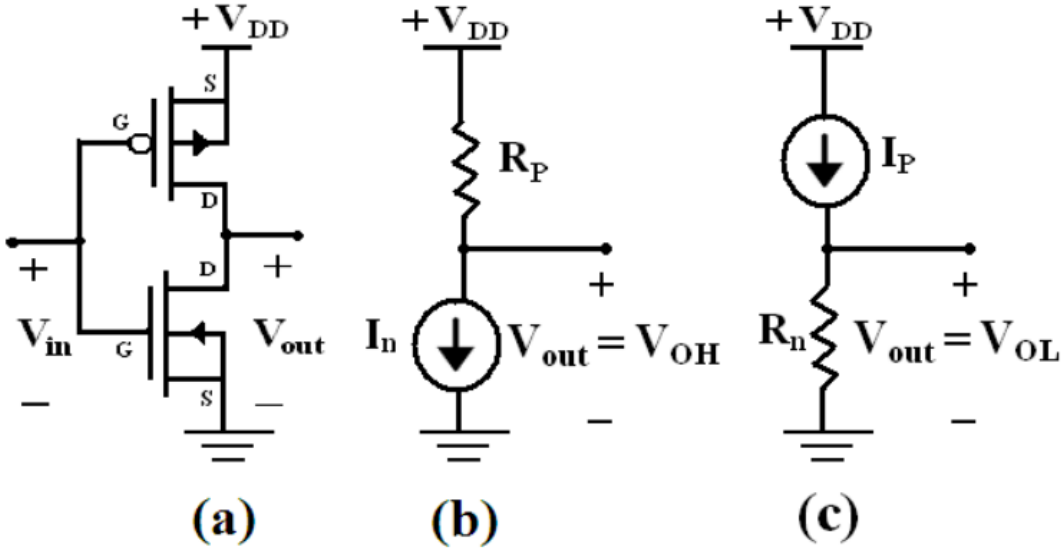

Fig. 3.1. (a) CMOS Inverter, Equivalent circuit for (b) „high“ input (c) „low“ input

TABLE 3.1 : 45nm CMOS PROCESS (Extracted at 270 C)

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Parameters	NMOS	PMOS
W/L	60nm / 80nm	120nm / 80nm
λ_{DS}	0.0832	0.058
m	1.51	1.5
β **(A)**	2.906E–010	1.042E–009
V_{TH0} **(V)**	0.3423	0.23122*
N_{sub} **(/cm^3)**	6.5E+0018	2.8E+0018
u_t	–1.1	–1.1

*V_{TH0} is the magnitude of zero-bias threshold.

3.3. DELAY MODELING OF CMOS INVERTER

Finding the delay for a square input pulse with zero transition time and then using an empirical correction technique to account for transition time is the basis for most previous analytical delay models [9]–[12], which diminishes the model's predictive nature and platform independence. In this work, we consider a pulse with a fixed rise and fall time, which is more realistic than earlier models. Since sub-threshold waveforms are extremely sensitive to process parameter fluctuations, supply voltage, and loads [20], we computed the propagation delay by properly dividing the input and output waveforms. VOH and VOL are considered as leakage current dominates at sub 90nm technology nodes, replacing "VDD" and "0" as output high and output low voltage. Finding High to low and Low to high propagation delays independently allows us to provide the most precise fully analytical model of the average delay of a sub-threshold CMOS inverter, accounting for all possible scenarios.

4. RESULTS AND STUDY

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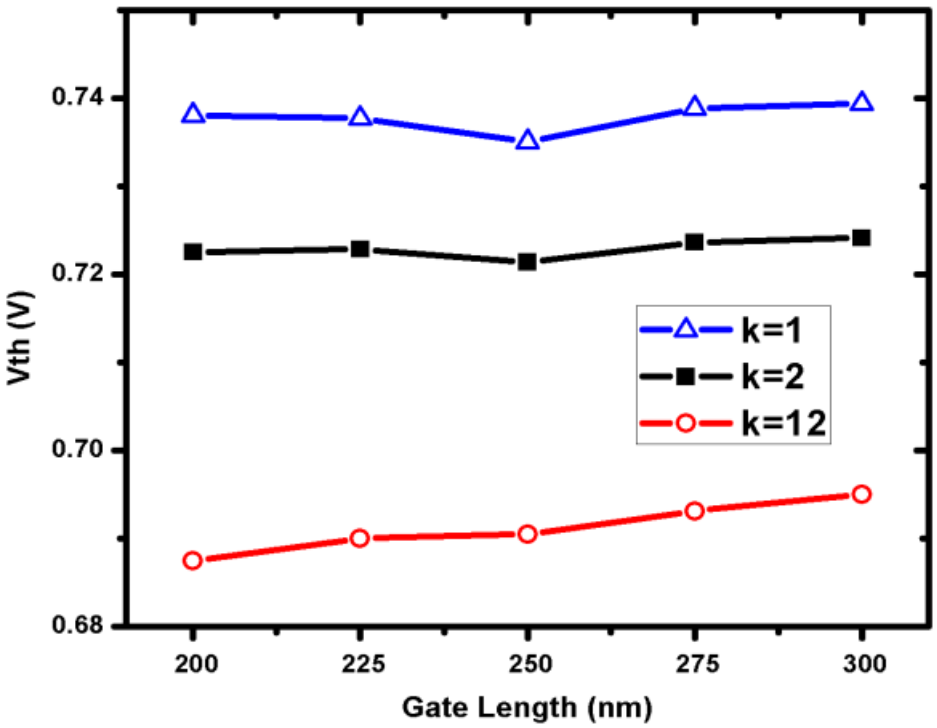

Fig. 4.1. Variation of threshold voltage for different gate length when the nanogap is filled by biomolecules having different dielectric constant, K=1, K=2 and K=12. Hence symbols and lines represent the simulated and modeled data respectively.

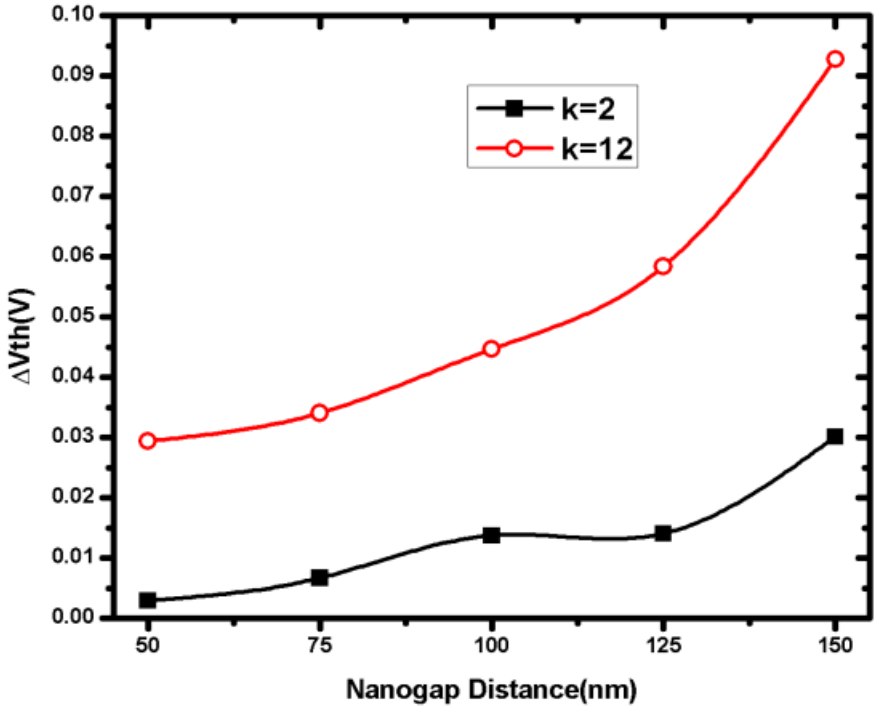

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Fig. 4.2.variation of ΔVT(VT,K=1-VT,K>1) for different nanogap length when the nanogap is filled by biomolecules having different dielectric constant, K=1, K=2 and K=12. Hence symbols and lines represent the simulated and modeled data respectively.

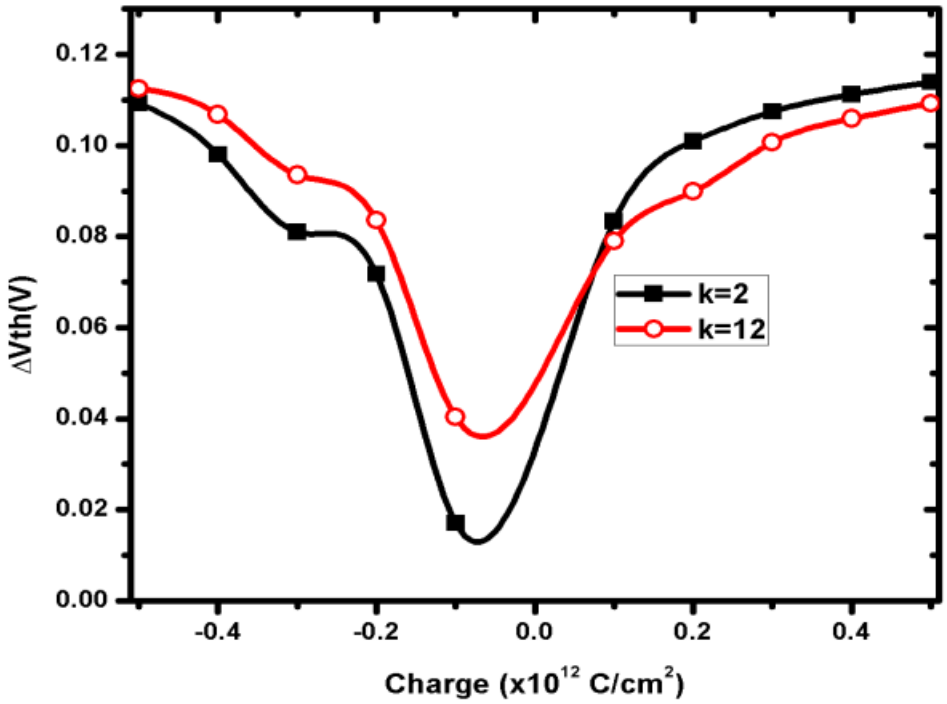

Fig. 4.3. Variation of ΔVT in presence of positive and negative charged biomolecules. Hence symbols and lines represent the simulated and modeled data respectively.

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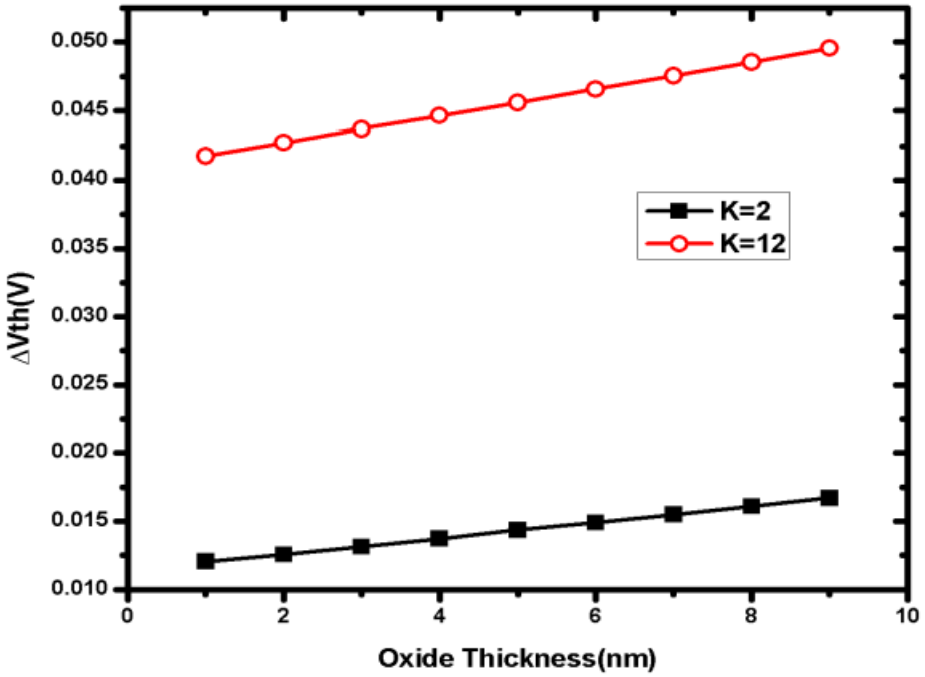

Fig. 4.4. Variation of ΔVT (VT,K=1-VT, K>1) for different oxide thickness when the nanogap is filled by the biomolecules of K=2 and K=12. Hence symbols and lines represent the simulated and modeled data respectively

CONCLUSION

In-depth consideration of low power design solutions is the primary focus of this study. The design principles discussed in the study are very applicable in many contexts where low power dissipation, rather than speed, is the primary priority. The power dissipation of the circuits has been minimised by considering both device and circuit level methods. In order to develop and implement ultra low power logic circuits, the switching power has been drastically reduced, putting the design into the sub-threshold region. However, high-speed operations are not possible with the sub-threshold method because the leakage current is the principal working current and has very lower magnitude. Still, low-speed low-power uses have been taken into account. The literature's first application of adiabatic logics in the sub-threshold zone helps to cut power dissipation even further. The switching and leakage power dissipation of adiabatic logic circuits in the sub-threshold regime can be greatly reduced.

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