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# Fully-Dynamic Noise Aware Three-Stage Low Power Comparator Using ERC

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## ABSTRACT

This proposed project presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by cancelling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the conventional two-stage and the proposed three-stage comparators are implemented in the same CMOS process. Measured results show that the modified version of three-stage comparator improves the speed. Further, this concept is enhanced by presenting a new energy-efficient novel voltage comparator, termed an edge-race comparator (ERC), in this article. It compares the differential input voltage by generating two propagating edges in two inverter loops and by measuring the distance between the two edges. The two edges race with each other and the winner is finally determined. The comparator is low power and low noise and does not require high-voltage headroom. It can automatically adjust its noise, power consumption, and delay according to the input voltage, thereby saving significant energy and time in coarse comparisons and reducing the noise in fine comparisons

**KEYWORDS:** kickback, Through, edge-race comparator, analogto-digital converters, central processing units, successive-approximation-register.

## 1. INTRODUCTION

Comparators are widely used in many applications such as voltage regulation, brown-out detection, and analog-to-digital conversion. In some of these applications, the performance of the entire circuit directly relies on the performance. A high-resolution successive-approximation-register (SAR) analog-to-digital converter (ADC) is a good example, which needs an especially low-noise comparison to distinguish voltages that are very close for fine

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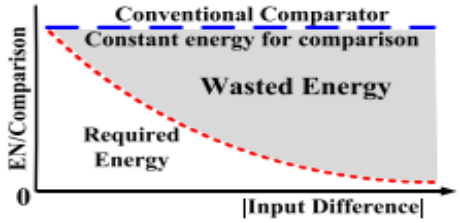
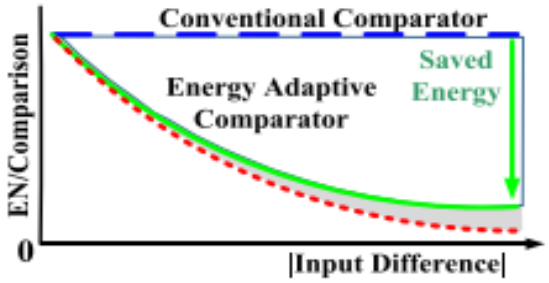
bit decisions requiring a large amount of energy that takes a significant portion of the total conversion energy.




(a)

Fig. 1. Required energy for comparison versus input difference. (a) Conventional comparators wasting most energy for large input difference.




(b)

(b) Energy scaling saved wasted energy for comparison. comparator's performance as the comparator plays a key role.

However, as depicted in Fig. 1(a), while the actual energy requirement sharply decreases as the input signal difference becomes larger, conventional clocked comparators [1]–[3] usually consume nearly constant energy for each comparison since they are designed according to the most accurate and power-hungry comparison. Therefore, in these kinds of applications, adjusting the energy for comparison according to the input difference level can greatly help in reducing the total comparison energy [Fig. 1(b)] as well as the overall energy consumption. For this reason, some prior works on SAR ADCs have presented techniques for comparator energy scaling [4]– [10], including dual ADC architectures that use two comparators for coarse and fine comparisons [4], [5], multiple repetitive comparisons for noise-critical bits [5]– [7], and time-domain comparators whose noise level can be modulated by changing the length of the delay lines [8]. However, these structures reduce the simplicity of the SAR structure by introducing overheads for extra control, increasing design and control complexity. They also have a limited number of energy scaling steps and a limited noise tuning range, making it difficult to benefit much from comparator energy scaling. In addition, some prior techniques require preprogrammed scaling by prediction, introducing additional inefficiencies from prediction misses. AS AN important analog module, the voltage comparator is widely used in various applications, such as analogto-digital converters (ADCs) [1]– [3], memories [4], and wireless sensor networks [5]. In such applications, low power is an important consideration, owing to the popularity of mobile, implantable, and wearable devices. For implementing low-power ADCs, the successive approximation register

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(SAR) ADC is the preferred architecture [6]–[9]. The SAR ADC depends on its comparator to achieve the target speed and resolution, but the comparator takes up a large portion (typically 50–60% [10]) of the total SAR ADC power budget. Specifically, a high-resolution SAR ADC requires a low-noise comparator to distinguish a small voltage difference at fine LSB decisions, leading to large power consumption at LSB decisions. More seriously, as shown in Fig. 1(a), a conventional comparator consumes almost constant energy at every bit decision (across the range of input voltage), because the comparator is designed according to the most power-hungry LSB decision. Nevertheless, the actual required energy at coarse MSB decisions (large input voltage) is much smaller, because, at coarse MSB decisions, the comparator noise does not need to be so small and the energy consumption does not need to be so large [see Fig. 1(a)]. This leads to wasted energy at coarse MSB decisions For this reason, many techniques have been proposed in recent years to realize energy scaling.

## 2. LITERATURE REVIEW

Jan Crols. et al. [1] (1994) have invoked CMOS Switched-Capacitor Circuits with low power consumption for operational amplifier. Switched opamp: it is focused on replacing the vital buttons with opamps which are enabled and disabled without having to use voltage multipliers. The main bottleneck problem in this proposed method is the lack of scalability with throughput. Andrew M. Abo., et al. [2] (1998) has been developed with the a0.6 µCMOS technology, 14.3 MS/s and 10-bit ADC, Analog to Digital Circuit. Two-phase, fully differential amp consists of a first stage folded-cascade followed by a second stage common source. Unfortunately, Density constraints are not reduced and the complexity parameter is very high in this process. Bosco Leung. et al [3] (1997) introduced Sigma-Delta Modulator with good performance, good baseband input and low power, working amplifiers. In the phase of a 1.2-m CMOS, a second-order passive sigma-delta modulator was produced. But, the lack of user-defined amplification and latency improvements are the main drawbacks of this content. S. J. Steyaert. et al [4] (1998) have established a differential modified, dynamic, 77-dB (16 kHz) bandwidth, and a 62 dB (signal-to-noise) peak ratio with a Sigma–Delta Digital Conversion Converter. The topology of modulators has been converted into half-time integration. Building blocks of dedicated low voltage circuit, such as an AB class operational transduction amplifier, a common-mode feedback amplifier and a comparator and low valuation design techniques will be processed. The current mode signal processing using CMOS technology has gained great interesting circuit designing. With the shrinkage of feature size and increasing demand of high speed and low power application, the current-mode circuit has been considered to be an alternative to voltage-mode circuit. Current comparator is fundamental component of analog system because of better accuracy, low noise and low power consumption. It can be used in A/D converters, oscillators, current to frequency converters, VLSI neural network, sensor circuit and portable wireless communication etc. H. Traff [1] proposed the first high speed, low input impedance current comparator using a simple inverter. Tarff's approach has been modified by a number of designs, A. T. K. Tang et al. [2] and L. Ravezzi et al. [3], where speed increases have been attained at the cost of an increase in power consumption. Several previous high-speed comparator designs have been proposed. In all [6] pre charged function block is attached to several feedback transistors which add extra discharge paths, thus reducing the comparator's delay. However, the precharge period is not utilized for any computation, so the design is not as fast as our high-speed design, as we will show in the sequel.

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## 3. EXISTING METHOD

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator, as shown in Fig. 4. Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages of Fig. 4(b) and extra paths M29–32 in the latch stage of Fig. 4(c). The extra first two stages use pMOS input pair

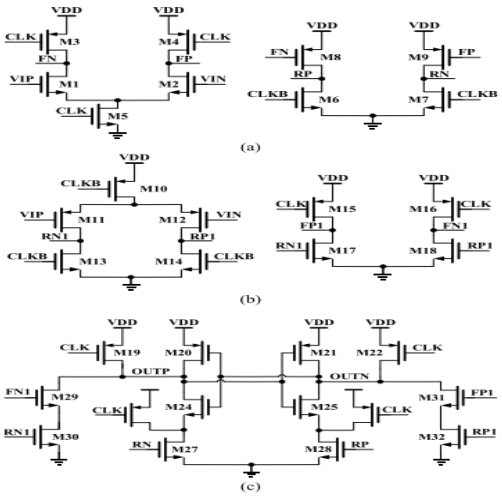


Fig. 2. Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further. The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 2(b) are reset to GND, while FP1 and FN1 are reset to VDD. This turns off M30 and M32 in Fig. 4(c), ensuring that there is no static current in the extra path M29–32. In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 4(b) rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 2(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 2(c) are turned off again to prevent the static current. Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, and lower kickback noise. It is suitable for high-speed high-resolution SAR ADCs. As an example, the proposed modified version is suitable for the time-interleaved noise-shaping SAR ADC in [13]. As pointed out in [13], its ADC speed is limited by the comparator speed, and its ADC resolution is limited by the comparator kickback noise. Although Zhuang et al. [13] use a channel isolation to reduce the influence of kickback noise, this isolation increases the complexity of

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system. By contrast, the proposed modified version of three-stage comparator can solve these issues. It has the fastest speed and the smallest kickback noise compared to other comparators.

## 4. PROPOSED METHOD:

### EDGE-RACE COMPARATOR:

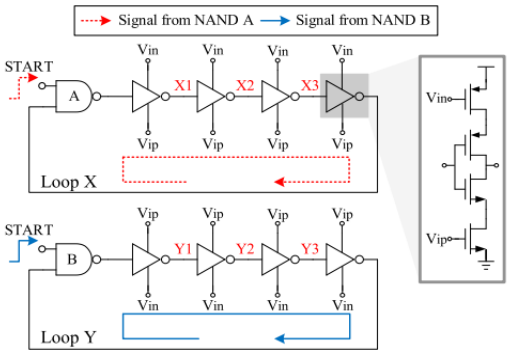


Fig.3 Proposed ERC.

Above Figure shows the proposed ERC. Its timing diagram is shown in above Fig, which will be explained later. Similar to the EPC in previous Figure, the proposed ERC also consists of inverter delay units and NAND gates. The delay of the delay units is also controlled by the comparator inputs Vip and Vin. The difference is that we separate the single loop into two loops, in order to increase the comparison speed and to reduce the interference between the two edges, as will be explained later. The operation of the proposed ERC is as follows. When START = 0, the two loops are in the reset phase. When START rises to 1, the two NAND gates generate two propagating edges in the two loops. The two edges start from the same starting line and race with each other, as shown in Fig. 3. They propagate in the two loops recursively. As time goes on, the distance between the two edges gradually increases, because they have different propagating speeds. Finally, when the distance exceeds a preset value d0, the race stops, and the winner (comparison result) is determined. This preset value d0 can be set to 2 inverter delays by using the circuit of Fig. 3(a), which will be explained later. If the edge in loop X is faster than loop Y, then we have Vip > Vin, and vice versa. In contrast, in the EPC of Fig. 2, the two edges start from different positions in the loop when START rises to 1.

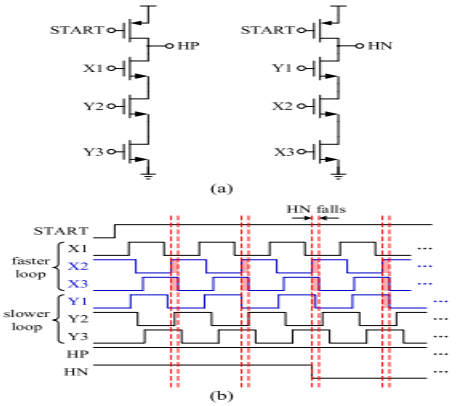




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Fig. 4. (a) Circuit for measuring the distance between edges and (b) timing diagram of Vip > Vin.

Thus, the initial distance between the two edges is equal to 5 inverter delays. As time goes on, this distance gradually decreases. When the distance decreases to 0, the comparison result is generated. Thus, we can conclude that, for the EPC of Fig. 2, the preset value d0 is 5 inverter delays. The major advantage of the proposed ERC is that it has a much faster comparison speed than the EPC. This is because the preset value d0 of the proposed ERC (2 inverter delays) is 2.5 times smaller than that of the EPC (5 inverter delays). Moreover, although Figs. 2 and 3 only show 8 inverter delay units for simplicity and easy understanding, there are actually more inverter delay units in real applications [17] (for example, we can use 16 inverter delay units for Figs. 2 and 3 each). In this case, the preset value d0 of the EPC becomes 9 inverter delays. In contrast, the preset value d0 of the proposed ERC is still 2 inverter delays, because we use an extra circuit [Fig. 4(a)] to ensure the fixed d0, which will be explained later. As a result, the speed of the proposed ERC is 4.5 times faster than the EPC in this case. To ensure the fixed d0, Fig. 4(a) shows the circuit for measuring the distance between the two propagating edges. It is as simple as two dynamic logics, which generate the comparison results HP and HN ("P" and "N" stand for positive and negative outputs, respectively). In the reset phase (START = 0), both HP and HN are reset to high ("H" stands for high). Meanwhile, both X1 X2 X3 and Y1 Y2 Y3 are reset to 010 through the NAND gates in Fig. 3. After START rises to 1, the comparator starts to work, whose timing diagram is shown in Fig. 4(b). As can be seen, the two propagating edges start from the same starting line [the initial phase difference between the two loops is zero in Fig. 4(b)]. Because Vip > Vin in this case, the propagating edge of loop X is

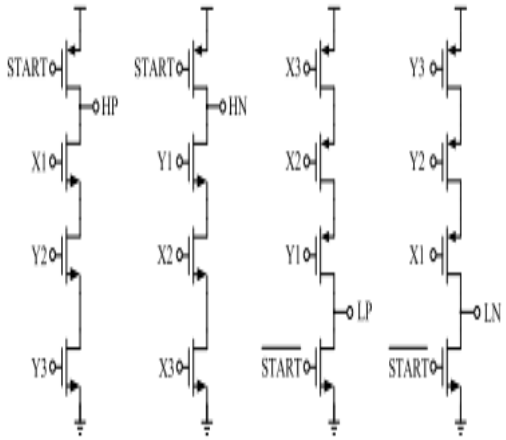


Fig. 5. Improved version of the circuit for measuring the distance.

slightly faster than loop Y, which causes the distance between the two propagating edges to gradually increase. When the distance is sufficiently large, X2 X3 Y1 become simultaneously high [see the red shaded regions in Fig. 4(b)], which pulls down HN. Meanwhile, HP remains high and does not change. These comparison results HP = 1 and HN = 0 match well with Vip > Vin. Here, the preset value d0 is approximately 2 inverter delays, because the comparison lasts until the edge distance increases to approximately 2 inverter delays. Let us look closely at Fig. 4(b): at the beginning, the falling edge of Y1 is the same as X1. Also, only X2 X3, not including Y1, are simultaneously high (the red shaded region). As time goes on, the falling edge of Y1 gradually enters the red shaded region, because loop Y is slower than loop X.

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This makes X2 X3 Y1 simultaneously high, leading to the end of the comparison. Because, at this moment, the distance between Y1 and X1 falling edges is approximately 2 inverter delays, we conclude that the preset value d0 is approximately 2 inverter delays. The circuit of Fig. 4(a) has a limitation that it can only detect the moment when X2 X3 Y1 are simultaneously high, but it cannot detect when X2 X3 Y1 are simultaneously low. To overcome this limitation, Fig. 5 shows an improved version of the circuit. The only difference between Figs. 4(a) and 5 is the addition of two extra dynamic logics for generating LP and LN. In the reset phase (START = 0), both LP and LN are reset to low ("L" stands for low). After START rises to 1, the circuit works similar to that in Fig. 4(a). The only difference is that it uses three pMOS transistors to pull up the output voltage LP or LN, rather than using three nMOS transistors to pull down the voltage as Fig. 4(a) does. This modification effectively detects the moment when X2 X3 Y1 are simultaneously low. Meanwhile, the HP and HN branches in Fig. 5 work in the same way as Fig. 4(a) for detecting the moment when X2 X3 Y1 are simultaneously high. To further improve the performance of Fig. 5, Fig. 6 shows the final version of the circuit. The only difference is two modifications. First, we add inverters I1–I6 to improve the driving ability and to make the edges sharper. Second, we add extra transistors M17–M20 to eliminate the glitches in HP, HN, LP, and LN due to coupling. The issue of glitches can be seen in Fig. 5: after START rises and before the comparison result is generated, we want HP, HN, LP, and LN remain unchanged. However, they are actually disturbed by the variation in X1–X3 and Y1–Y3 through the coupling of parasitic capacitances, because HP, HN, LP, and LN are floating at this moment in Fig. 5. To address this issue, we add

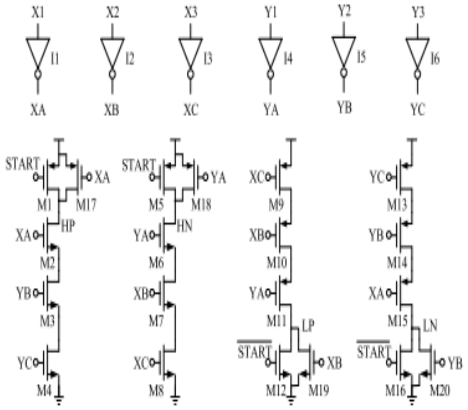


Fig. 6. Final version of the circuit for measuring the distance

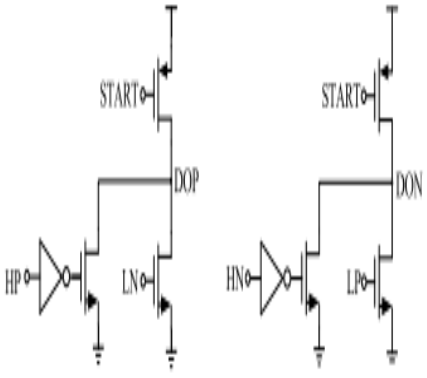

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Fig. 7. Circuit to obtain the final comparison result. extra transistors M17–M20 into Fig. 6 to effectively reduce this disturbance.

Fig. 7 shows the circuit for storing the comparison results. It is based on a conventional dynamic register circuit of [18] with one modification. Two nMOS transistors, rather than only one nMOS, are used in each branch, because we need to combine the four results HP, HN, LP, and LN. Here, HP and LN are combined to generate the final result DOP, and HN and LP are combined to generate the final DON.

## 4. RESULTS

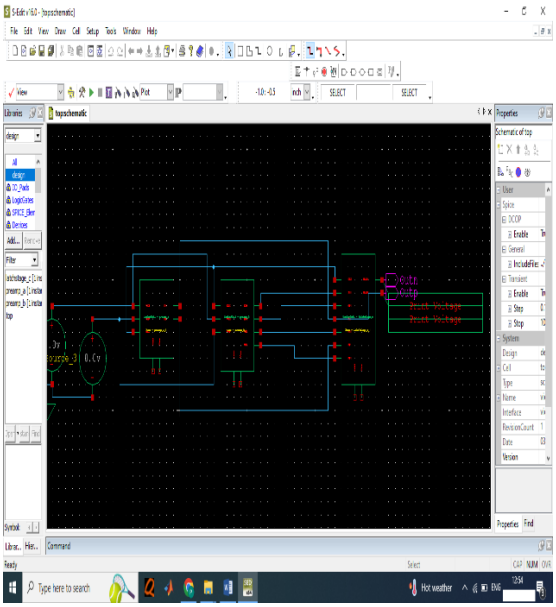

Fig:8 proposed block diagram

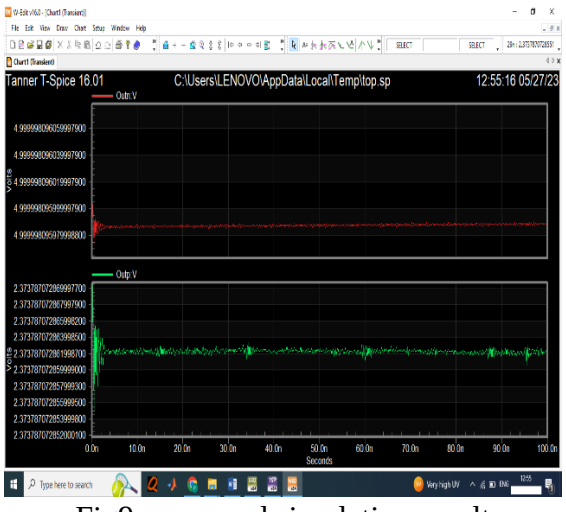


Fig9: proposed simulation result

## 5. CONCLUSION AND FUTURE SCOPE

This article proposes a novel voltage comparator for low power high-resolution SAR ADCs. Compared to a recently reported method, the proposed comparator speed is significantly



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increased, and the power consumption is greatly reduced. The simulation and measurement results validate the proposed structure. In the future one can reduce the input referred latch offset voltage, power consumption, Hysteresis response. Offset voltage optimization and optimization of the circuits after layout can be one topic. Finding application specific comparators can be another topic.

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