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DESIGN AND IMPLEMENTATION OF ALU USING GDI WITH CLOCK GATING TECHNIQUE

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Abstract:

In the area of VLSI, circuit complexity is rapidly multiplying together with reducing chip size and the IC ‘s produced today are highly sophisticated. It is the period of growing technology and scaling of devices nanometer experiment. This project describes the design and implementation of ALU using GDI with Clock gating technique. Low-power ALU design is made possible by the minimal digital cascaded design technique known as GDI, which reduces power consumption and propagation delay. Clock gating is a power saving technique used to reduce the power consumption of digital circuits by disabling the clock signal that are actively not in use at different parts of the circuit. When compared to CMOS transistors, the number of GDI transistors is reduced to half. As a result, when compared to CMOS, power and area are reduced. The power efficiency is 92%, area efficiency is 50.4% and delay efficiency is 11.3%. In comparison to previous CMOS, PTL, GDI approaches, the simulation demonstrates that the layout is more effective with less power usage, less area, and faster performance. Tanner's EDA tool uses 45nm technology for the design an d analysis.

Key Words: ALU (Arithmetic and logic unit), GDItechnique, Clock gating, Full Adder, Power, Area, Delay, VLSI (Very Large-Scale Integration), Efficiency.

• INTRODUCTION

As digital technology continues to advance, there is a swift rise in demand for high speed and low power consumption. With the reduction of contemporary CPUs are combined with a vast number of transistors on a single chip, regardless of transistor size. A higher level of integration results in larger circuits and more power usage. The semiconductor industry is very concerned with developing low power, high speed circuits for manufacture due to rapid integration. A functioning block of digital circuitry is formed by the ALU, [8]. These are complicated combinational circuits which conduct arithmetic and logical operations.

The Arithmetic and Logic Unit (ALU) is one of the most important logic building blocks in any processor design. The ALU's area suitability and functional efficacy will have an impact on the processor's overall performance. ALU block power consumption has an impact on the processor's overall power dissipation. In order to boost the ALU's speed while reducing power dissipation, a very well design is required.

A wide variety of complicated logic functions could be implemented in GDI cells with just two transistors. The GDI approach is appropriate for designing quick, low-powercircuits with fewer transistors than CMOS, while increasing power characteristics and enabling straightforward Shannon's theorem-based design employing tiny cell libraries. This study's objective is to look at a typical situation in order to interpret and explain its GDI approach in comparison to CMOS technique. This project serves as an example of the GDI technique's

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application to ALU design. This work uses the GDI approach to design an ALU.

- **LITERATURE REVIEW**

M. A. Ahmed and M. A. Abdelghany, have implemented Low power 4-Bit Arithmetic Logic Unit using Full-Swing GDI Technique[3]. The main issues in the electronics industry are power dissipation and circuit area. They provided a design of 4-Bit Arithmetic Logic Unit (ALU), which is considered an effective method for low power digital design while reducing the area of the circuit compared to other logic styles. They proposed an ALU design that included a 2x1 Multiplexer, a 4x1 Multiplexer, and a low power Full Adder cell to performarithmetic and logic operations. Swing restoration circuits were used to boost the output of the GDI cells. They proposed the Modified-GDI approach, in which the NMOS and PMOS transistors' substrate terminals were permanently connected to GND and VDD, respectively. This modification enables the fabrication of GDI cells in standard CMOS processes, which are less expensive than twinwell and (SOI) processes. The simulation is performed using Cadence Virtuoso on a 65nm TSMC process, demonstrating that their design consumes less power while achieving full swing operation when compared to previous work.-2018

Amanpreet Kaur, Jyoti Saxena, Ravneet Kaur have comparatively analyzed a GDI based D flip-flop circuits using 90nm and 180nm[4] technology. Using a supply voltagebelow the threshold voltage while running the circuit is a strategy for achieving ultra-low power. Operating digital circuits in the sub-threshold region results in extremely low power consumption. The GDI (Gate Diffusion Input) approach is the foundation of the sub threshold circuit. The DFF architecture permits lowering the power-delay product and circuit size while preserving a simple logic design. With regard to gate size, number of devices, delay, and power consumption, performance comparison with other DFF design methodologies is shown, highlighting the benefits and shortcomings of GDI DFF in comparison to other approaches.

In order to create a high performance processing element forVLSI systems, a D-flip-flop is proposed. – 2016

Biswarup Mukherjee, Aniruddha Ghosal have designed & studied a low power high speed full adder using GDI multiplexer[5]. Most digital circuit designs, including digital signal processors (DSP) and microprocessor data path units, rely on the binary adder. As a result, extensive research is still being conducted to improve the power delay performance of the adder. As it decreases area and delay in comparison to other switch types, MOS switches are utilised in PTL-based VLSI devices to transmit distinct logic values in multiple node sites. It decreases the quantity of MOS transistors utilised in the circuit, but it has a significant flaw in that the output voltage levels are no longer equal to the input voltage levels. A series transistor's output voltage is lower than its input voltage. This project also proposes a new method for realising a low power full adder using a set of Gate Diffusion Input (GDI) cell-based multiplexers. A full adder is a common example of a combinational circuit that is widely used in Application Specific Integrated Circuits (ASICs). Using a cutting-edge simulation tool, the projected method outperforms a general CMOS-based full adder in terms of behavioural performance. - 2015

Madhusudhan Dangeti and S.N.Singh have used a GDI technique for the minimization of transistors Count and Power by realising the digital circuits'[6] technology has scaled down to nano regimes in response to efforts for low power, high speed embedded systems, allowing

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for increased chip density, i.e., more functionality to be integrated on a single chip. Apart from the traditional CMOS design style, these efforts resulted in several different design techniques, one ofwhich is GDI. GDI is essentially a technique for designing fast, low-power circuits with a smaller number of transistors than traditional CMOS design and existing PTL techniques. Various combinational circuits were implemented, including multipliers using 0.5m that reduced power by up to 40% andcomparators using 1.6m that reduced power from 1.82(mW) to 1.41(mW). The D-flip flop was also implemented using 0.35m and 0.18m at 3.3 V and 1.8V, with 812.7W and151.7uW consumed, respectively.-2012.

- **EXISTING SYSTEM**

Using the gate diffusion input (GDI) design technique, fewer transistors are required to implement a given logic function in digital integrated circuits. This technique is crucial for modern VLSI design since it can result in significant reductions in size, power consumption.

Each logic gate in conventional CMOS logic architecture needs a minimum of four transistors, two transistors for each pull-up and pull-down network. A single transistor coupled toa diffusion region as well as a gate diffusion input (GDI) is used to implement each gate in the GDI architecture, though. The behaviour of the transistor is managed by the common GDI area, which is coupled to several gates.

The input signals are converted into diffusion inputs in GDI design, which are then employed to regulate the behaviour of the transistor. Connecting various inputs to a single diffusion region produces the diffusion inputs. The GDI area, which regulates the gate voltage of the transistor, is thenlinked to this diffusion region.

Because it enables the implementation of numerous gatesusing a single transistor, the GDI technique is an extremely effective method for decreasing the quantity of transistors in a circuit. Significant reductions in space, power use, and latency may result from this. The body effect and other problems thatcan occur in conventional CMOS gates cannot affect GDI gates because they are implemented utilising a single transistor [7].

Flexibility is one of the main benefits of GDI design. A variety of logic operations can be implemented with a relatively minimal number of transistors because of GDI region is shared by several gates. Moreover, many input logic gates can be implemented without the requirement of extra transistors so because input signals are converted into diffusion inputs.

The Gate-Diffusion-Input (GDI) shown in Figure 1 is an approach based on the use of a straight forward cell, as shown in Fig. 3.1 At first glance at this circuit, one may assume a CMOS inverter; however, there are a few significant distinctions between the two: (1) The GDI cell has three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Unlike a CMOS inverter, NMOS and PMOS may be flexibly biased since their major portions are coupled to N or P, respectively.Fig. 1 depicts the standard GDI cell.

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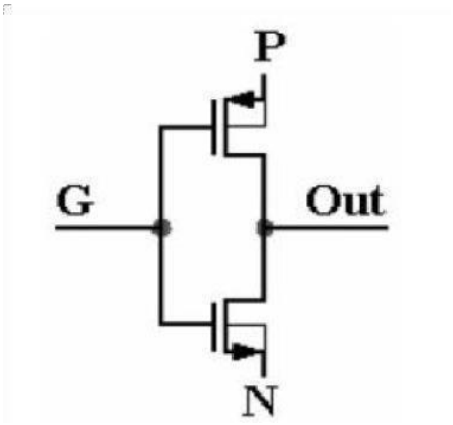

Fig. 1: Basic Gate-Diffusion-Input cell.

TABLE 1: Functions of the basic GDI cell

Sr. No.	Input			Output	Function
	P	G	N		
1	B	A	0	$A'.B$	F1
2	1	A	B	$A' + B$	F2
3	B	A	1	$A + B$	OR
4	0	A	B	$A.B$	AND
5	B	A	C	$A'.B + A.C$	MUX
6	1	A	0	A'	NOT

Using merely various combinations of the inputs G, P, and N, the GDI cells with four terminals may be identified as a novel multi-functional device that can do six tasks. Table 1 demonstrates how minor configuration adjustments to the basic GDI cell's outputs G, P, and N can result in radically different logical functions at the input Out. In CMOS, most of these functions are complicated (often requiring 6–12 transistors), but in the GDI design approach, they are quite basic (only requiring 2 transistors per function). Several GDI cells can be combined to create multiple-input gates.

- **PROPOSED METHOD**

An Arithmetic Logic Unit (ALU) is a fundamental component of a computer processor that performs arithmetic and logical operations on binary numbers. The ALU is responsible for carrying out the basic arithmetic functions, such as addition, subtraction, multiplication, and division. It also performs logical operations such as AND, OR, and NOT, as well as comparison operations such as greater than, less than, and equal to. The ALU is made up of several sub- components, including the arithmetic circuits, logic circuits, and control circuits. The arithmetic circuits perform mathematical operations on two binary numbers, while the logic circuits perform logical operations on the input bits. Thecontrol circuits manage the flow of data within the ALU andensure that the correct operation is performed.

The speed and efficiency of an ALU are crucial to the overall performance of a computer system. Many modern processors have multiple ALUs, allowing them to perform multiple operations simultaneously and greatly increasing their processing power. The ALU is a key component of the central processing unit (CPU), which is responsible for executing instructions and performing calculations in a computer. Overall, the ALU plays a critical role in the operation of a computer processor, performing the basic arithmetic and logical

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operations necessary for the processing of data. Its efficiency and speed have a direct impact on the overall performance of the computer system.

In this project we will discuss two important components of digital electronic circuits - the Arithmetic Logic Unit (ALU) and clock gating. The ALU is a crucial component of a computer processor that performs basic arithmetic and logical operations on binary numbers, with multiple sub- components including arithmetic, logic and control circuits. The speed and efficiency of the ALU are vital to the performance of the overall computer system, with many modern processors featuring multiple ALUs to increase processing power.

On the other hand, clock gating is a power-saving technique used in microprocessors and other complex logic circuits that controls the clock signal to selectively enable or disable clock signals to unused parts of the circuit. By reducing power consumption in this manner, unnecessary clock signals are eliminated, allowing for energy efficiency without compromising circuit functionality. Clock gating can be implemented in various ways, with some modern microprocessors using advanced techniques that dynamically adjust the clock signal based on the processor's workload.

Overall, both the ALU and clock gating are essential components of digital electronic circuits, with the ALU performing crucial mathematical and logical operations and clock gating reducing power consumption in microprocessors and other complex logic circuits. The clock signal to a block of logic is controlled by a multiplexer in latch-free clock gating shown in Figure 2. The gated clock signal or an ungated clock signal is selected by the multiplexer. The control signal that specifies when the clock should be gated is ANDed with the original clock signal to produce the gated clock signal. The original clock signal is what is known as the ungated clock signal. Because a latch causes no delay, using a multiplexer instead of one eliminates the possibility of clock skew. The AND gate that is used to generate the gated clock signal adds a small amount of delay, although this delay is not as problematic as clock skew. Clock gating is accomplished by using an AND gate to combine the clock signal with a control signal to create a gated clock that is then applied to other circuit components. The control signal determines which module should receive the gated clock.

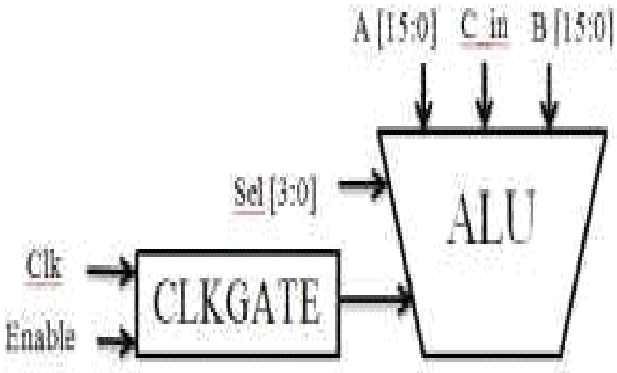

Fig. 2: Latch-free Clock Gated ALU design

BLOCK DIAGRAM

In this proposed method we are going to use a latch free clock gating technique in which a multiplexer is used is shown in Figure 3. The multiplexer contains selection lines which selects any inputs and route to a single output based on the control inputs. The operations performed by an ALU are arithmetic and logic operations which are mentioned below. These operations are performed based on the selection lines of a multiplexer as shown

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below.

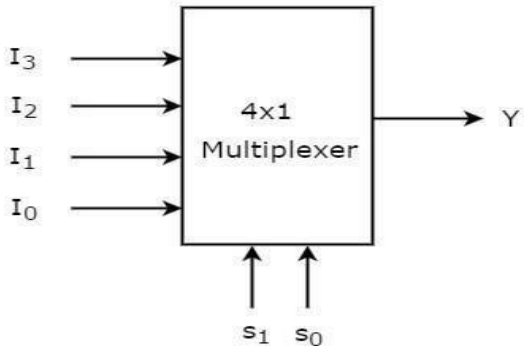

Fig. 3: Block diagram of 4x1 MUX

4X1 multiplexer has 4 i/p's i.e., I0, I1, I2, I3 and produces one o/p based on the selection lines S0, S1 is shown in Figure 4. And simulation results are shown in Figure 5,6,7,8.

Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

So, final equation,

Y = S0'.S1'.I0 + S0'.S1.I1 + S0.S1'.I2 + S0.S1.I3

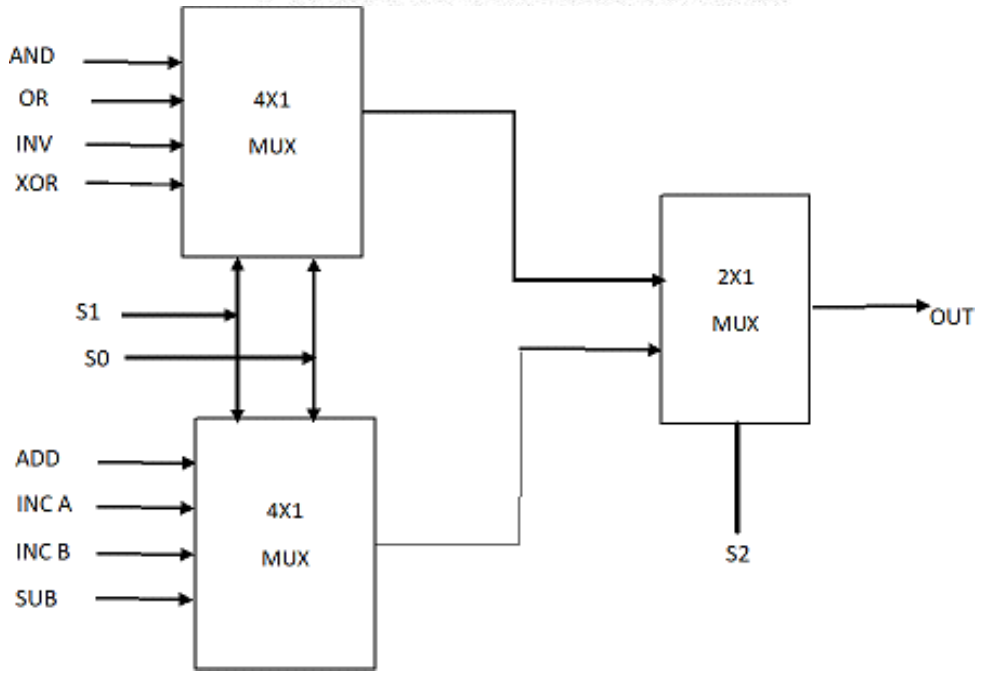

Fig. 4: Operations of an ALU using multiplexers

In this block diagram, we used two 4X1 multiplexers one 2X1 multiplexer. AND, OR, INVERTER, XOR are the inputs of logic unit. Based on the selection lines it can produce outputs as shown in the table below.

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Table 2: Functions based on selection lines

S2	S1	S0	FUNCTION
0	0	0	AND
0	0	1	OR
0	1	0	NOT
0	1	1	XOR
1	0	0	ADDITION
1	0	1	INCREMENT a
1	1	0	INCREMENT b
1	1	1	SUBTRACTION

The values of S0, S1, S2 should be given initially in a vertical format rather than horizontal format.

- The logical operations include AND, OR, NOT (INVERTER) and XOR.
- The arithmetic operations include Addition, Subtraction, Increment.

- **SIMULATION RESULTS AND COMPARISON**

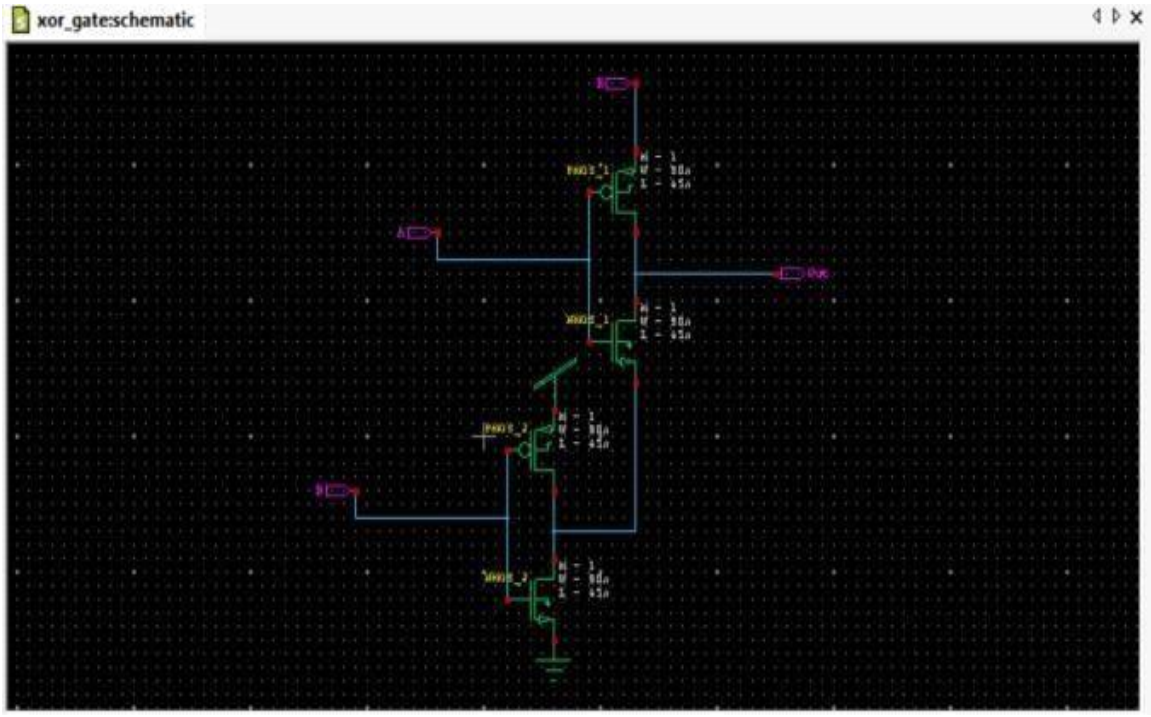

Fig. 5: Schematic design of XOR gate

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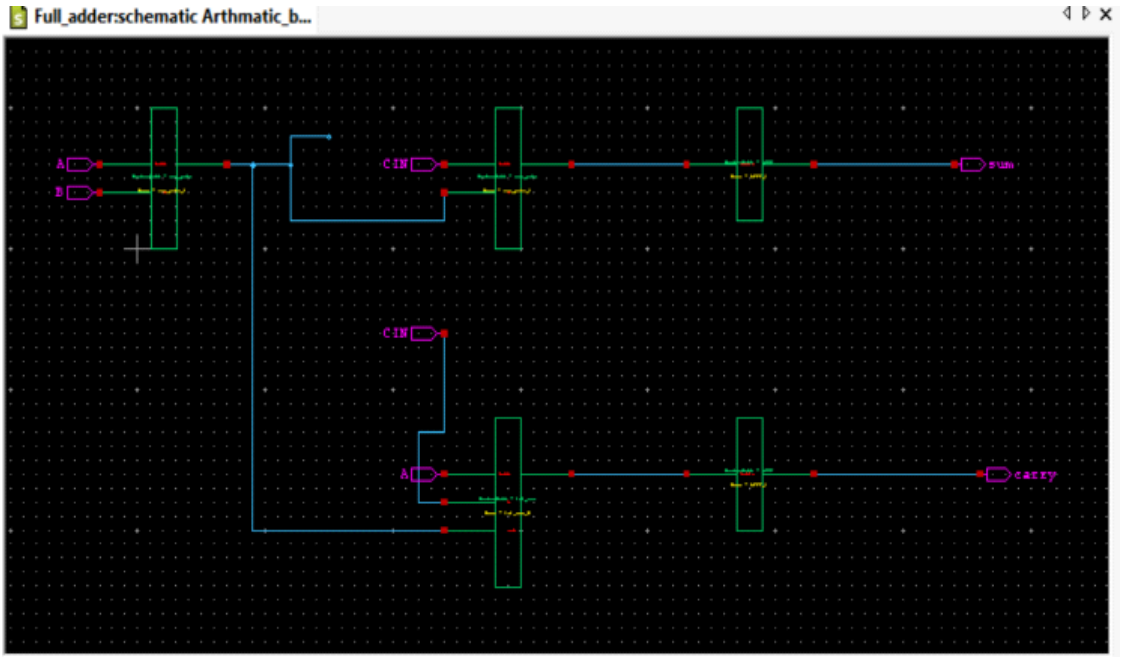

Fig. 6: Schematic design of Full Adder

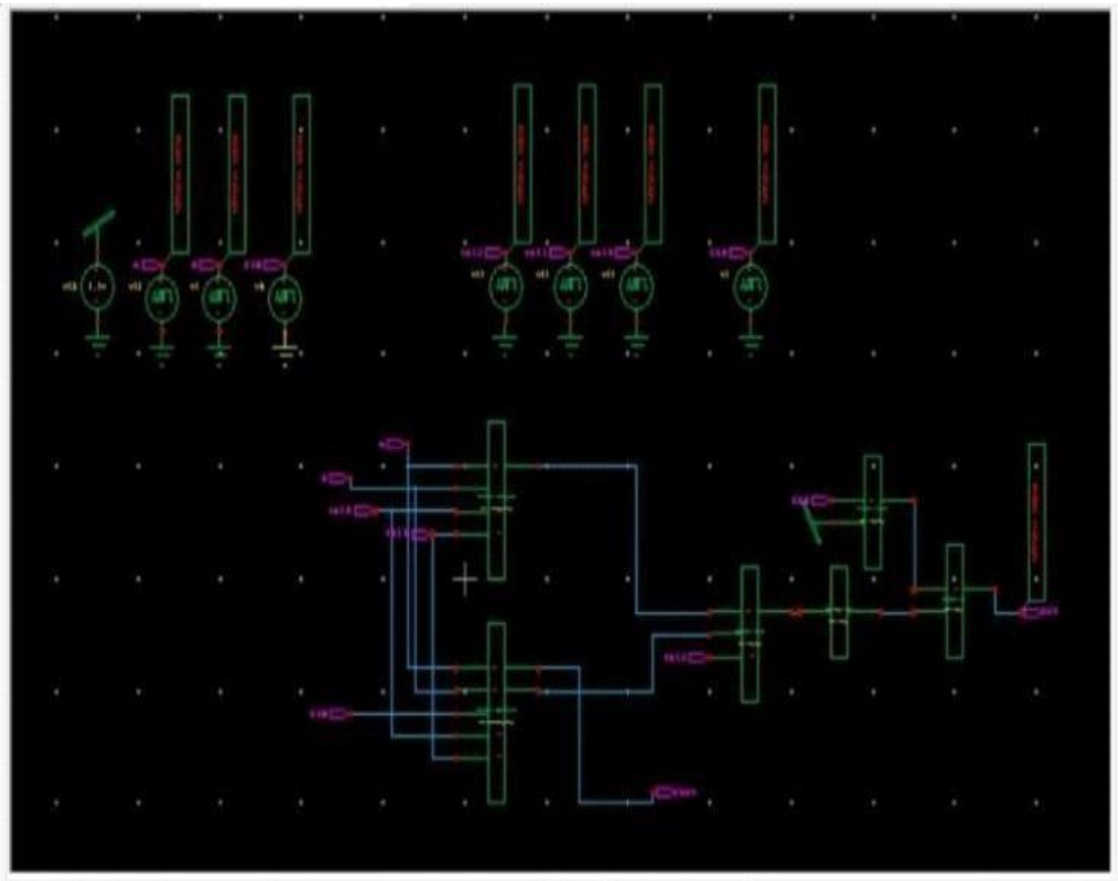

Fig. 7: Schematic design of 1-bit ALU with clock gating

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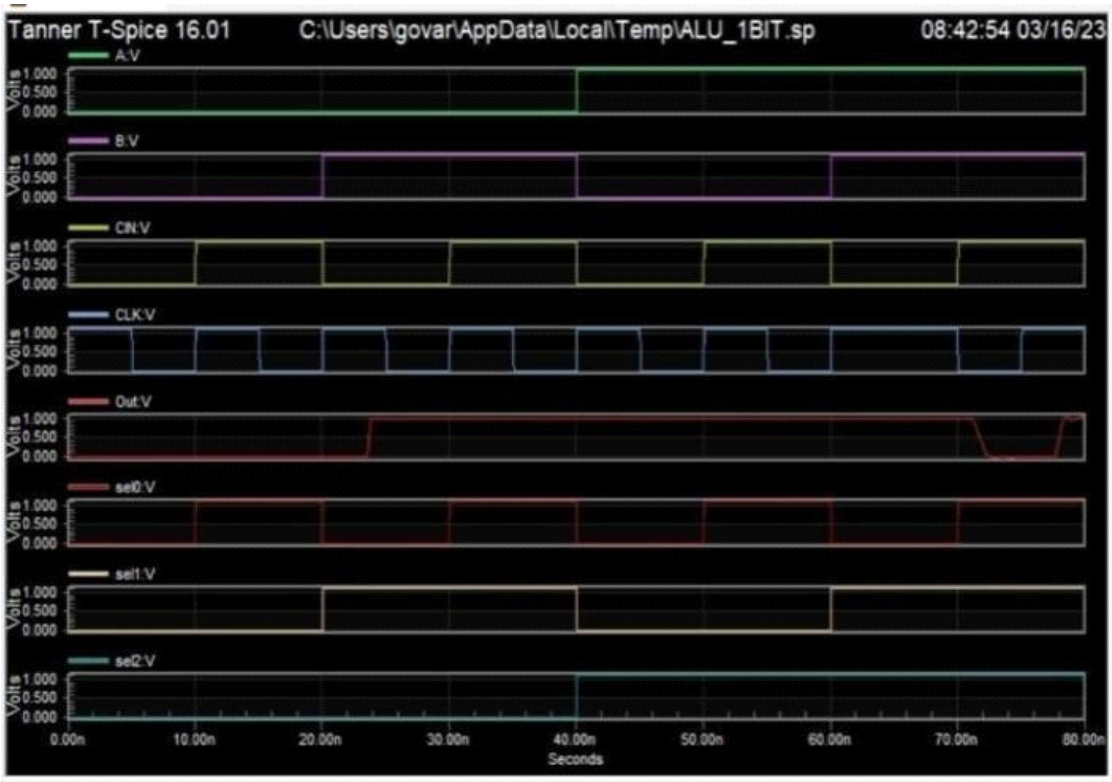

Fig. 8: Simulation waveform of 1-bit ALU with clock gating

Table 4: Average power comparison

Technique	**Transistor** Count	**Power**	**Delay** (ns)	**Power Delay Product**(pJ)
CMOs	384	5.18mw	50.71	262.88
PTL	320	3.66mW	37.236	136.28
GDI	248	65.65uW	25.21	1.655
GDI withclock gating	123	5.08uW	22.34	0.13

Table 5: Average power comparison

Sl. NO.	**Operation**	**ALU With OutClock Gating(Um)**	**ALU With Clock Gating (Um)**
1	AND	4.3	4.07
2	OR	4.19	3.9
3	NOT	4.42	4.37
4	XOR	5.1	4.8
5	ADDITION	4.63	4.39
6	INCREMENT A	4.19	3.9
7	INCREMENT B	4.58	4.66
8	SUBTRACTION	5.31	5.17

- **CONCLUSION**

Finally, in this study it is to be noted that the design and implementation of ALU using GDI with Clock gating technique have been performed with 45nm technology. A low power digital combinational design technique called GDI (Gate diffusion input) has been

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used. This technique allows for lower power consumption and shorter propagation delays in low-power ALU designs. Clock gating technique isalso used, which is a prominent approach employed in many synchronous circuits to reduce the dynamic power dissipation. The simulation shows that the design is more efficient than CMOS, PTL, GDI techniques in terms of power consumption, area, and delay. This project has been performed by using Tanner EDA tool with 45nm technology.

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