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# Comparison of 9-level switched capacitor based multilevel inverter with conventional 9-level CHBMLI:

**Arti Saxena Phd research Scholar[1]**
**Sangam University, Bhilwara, Rajasthan**
**Dr. Vinesh Agarwal[2]**
**Dept. of Electrical Engineering Sangam University, Bhilwara Rajasthan**

**Abstract:** This manuscript presents the comparison of 1-ϕ 9-level cascaded H-bridge multilevel inverter and 9-level Switched capacitor based multilevel inverter. To cheer the quality of inverter's output parameters primarily THD and switching losses, multicarrier phase shifted technique is consider for controlling the gate pulse of 9-level inverters and the complete analysis of THD for 9-level is done. This work is performed and results are validated using MATLAB/SIMULINK.

**Keywords**: Multilevel Inverter (MLI), Cascaded H-Bridge (CHBMLI), Multicarrier pulse width modulation technique (MCPWM).

## INTRODUCTION:

Now a days in the field of medium voltage and high power applications multi level voltage source inverter (VSI) playing vital role; as it has better waveform quality, low dv/dt stresses on switching devices and no electromagnetic interferences problem compared to conventional two level voltage source inverter [1].In many practical applications a sinusoidal voltage becomes necessity; owing to cost effectiveness of multi level inverter became popular choice as it generates staircase voltage closer to sinusoid, also as the number of levels increases waveform quality improves and the filter requirement reduces [2]. Basically, there are three classes of multi level inverter as a) Neutral/diode clamped multi level inverter, b) flying capacitor multi level inverter, c) cascaded H-bridge multilevel inverter (CMLI) [3]. For same voltage level, cascaded H-bridge inverter requires less number of switching devices, reduced voltage unbalancing problem [4-5]. There are various methods of modulation technique to minimize the Total Harmonic Distortion (THD) and to control the output voltage of multilevel inverter; carrier based PWM is one of them [6-8]. It is a so called sine triangle PWM; as a reference is sine wave and carrier is triangular wave. phase shifted

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method is a type of sine PWM technique. In this paper simulations of 9-level inverters is compared using phase shifted PWM technique for single phase, and there THD is analyzed.

**INVERTER TOPOLOGIES:**

**1. 9-level based conventional multilevel inverter:**

Fig. 1 deprived the basic layout of CHBMLI for single phase. Every splitting voltage source ($V_{dc1}$, $V_{dc2}$, $V_{dc3}$) associated in cascade through additional supply via a unique H-bridge circuit linked through it. Every circuit contains four switches that can create the voltage output source in positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit [3, 4].

The level of output can be given by

$$N_{level} = 2S + 1 \qquad (1)$$

Where, $S$ is the H-bridge

The voltage at every phase can be calculated by

$$V_{si} = 1V_{dc} (i = 1,2,3 \ldots) \qquad (2)$$

The number of switches used in this topology is given by the equation,

$$N_{switch} = 4S \qquad (3)$$

The rewards of the CHBMLI are series H-bridges for modularized outline and wrapping. The Fig 2 demonstrates the waveform of voltage output for a 9-level CHBMLI [30, 37].

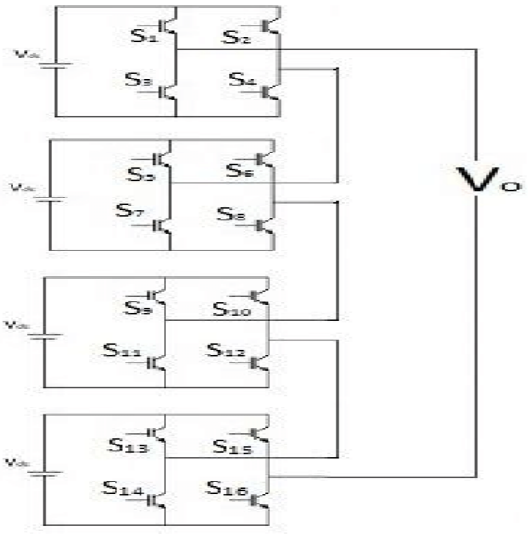


Fig 1: Topology for CHBMLI

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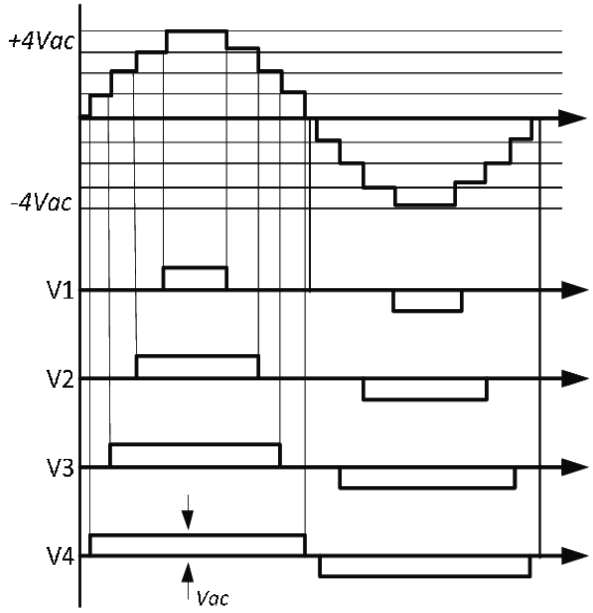


Fig 2: Typical Output Waveform for CHBMLI

## 2. 9-level switched capacitor based multilevel inverter:

Fig.3 shows the circuit topology of nine-level inverter, where *S*1, *S*2, *S7* , *S8* as the switching devices of SC circuits are used to exchange the connection of *C*1 and *C*2 in series or parallel ways. *S*3, *S*4, *S*5, *S*6, *S*9, *S*10, *S*11, *S*12 are the switching devices of cascaded H-Bridges. *Vdc*1 and *Vdc*2 are input PV voltages respectively. *D*1 and *D*2 are diodes to restrict the current direction. In this topology that backend circuit of this inverter is cascaded H-Bridges in series connection. H-Bridge is significant enough to ensure the circuit conducting regardless of the directions of output voltage and current. In the case of either inductive or resistive load, H-Bridge has four conducting modes, i.e., forward conducting, freewheeling, reverse freewheeling and reverse conducting.

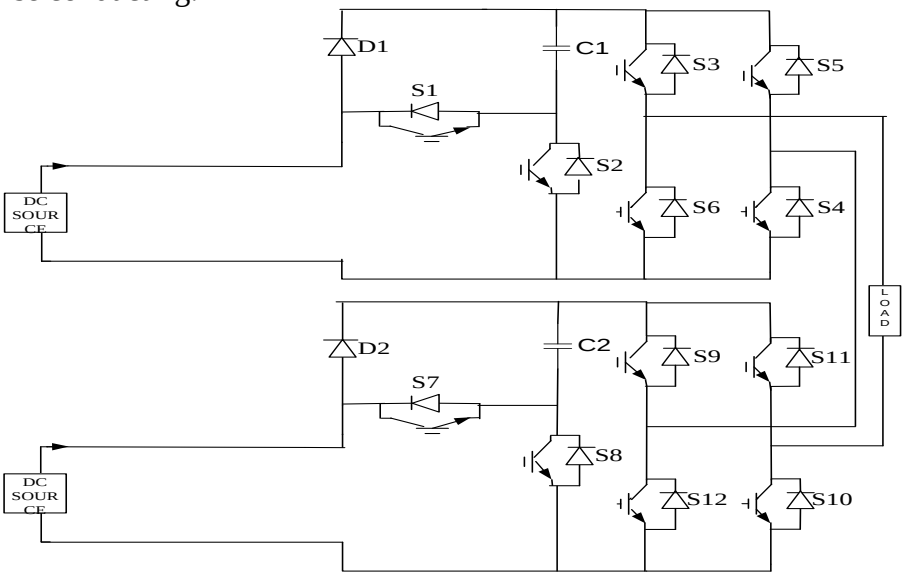


Fig. 3. Circuit topology of cascaded nine-level inverter (*N*1 = 2, *N*2 = 2).

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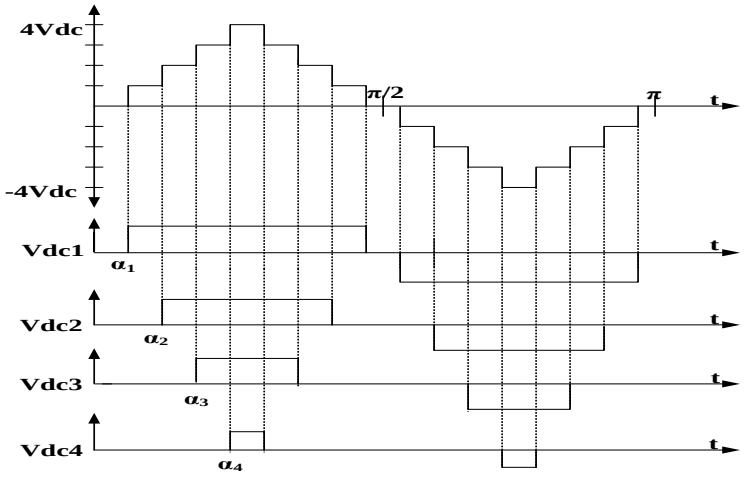


Fig. 4: Staircase output of 9-level SCMLI.

**Phase Shifted PWM (PS PWM)**

This technique is also called hybrid PWM technique and is used to generate the stepped multilevel output voltage waveform with lower % THD. Multilevel inverter with m levels requires (m-1) triangular carriers. All the triangular carriers have same frequency and have same peak to peak amplitude. The two carriers above zero have 180$^o$ phase shift between them. The same is true for the two carriers below the zero. In case, the number of converter levels is higher, the carrier waves are phase shifted accordingly, that is 120$^o$ for a 7-level system and 90$^o$ for a 9-level system and so on[8]. The dominant harmonics are concentrated around multiples of (m-1)/2 of the carrier wave frequency. This technique shifts the phase of every carrier in an accurate angle to diminish the harmonic content of the voltage output. The PSPWM suggest an even power allocation amongst cells. The smallest voltage output deformation is attained with 180/ N phase shifts flanked by the carrier [9,10].

Here, N is the number of single phase inverters.

$$\theta = \frac{360}{(m-1)} \qquad (4)$$

**SIMULATION AND RESULTS:**

1. **9-level Cascaded H-bridge Multilevel inverter:**

   Conventional 9-level CHBMLI is designed with the help of four H-bridge inverters comprises of 4 DC Batteries, 16 switches producing 9 level output voltage.

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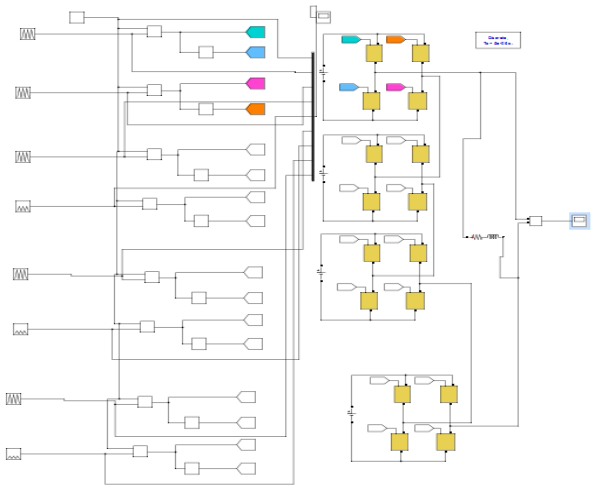

Fig. 5: 9-level Cascaded H-bridge Multilevel inverter:

## 2. Switched capacitor based 9-level multilevel inverter:

Switched capacitor based multilevel inverter is designed with the help of two capacitor and 12 switches comprises with two DC battery producing 9 level voltage output.

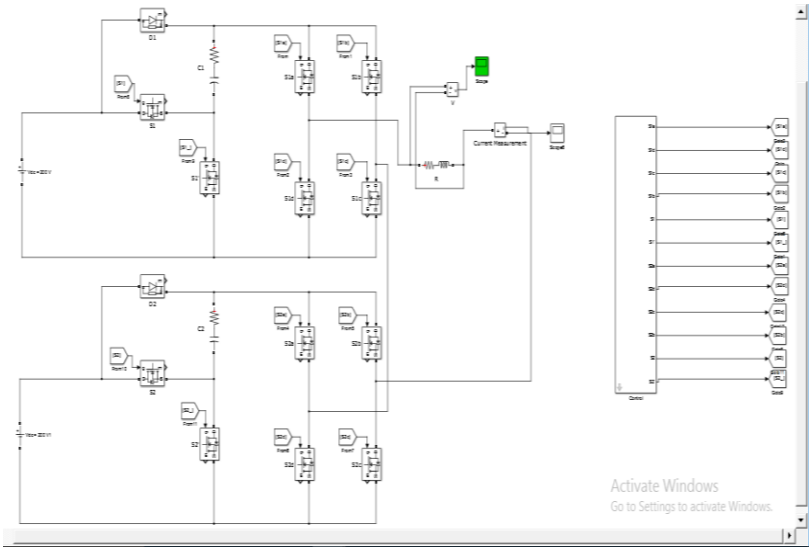


Fig. 6: Switched capacitor based 9-level multilevel inverter simulation

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## 3. Output of Conventional 9-level CHBMLI:

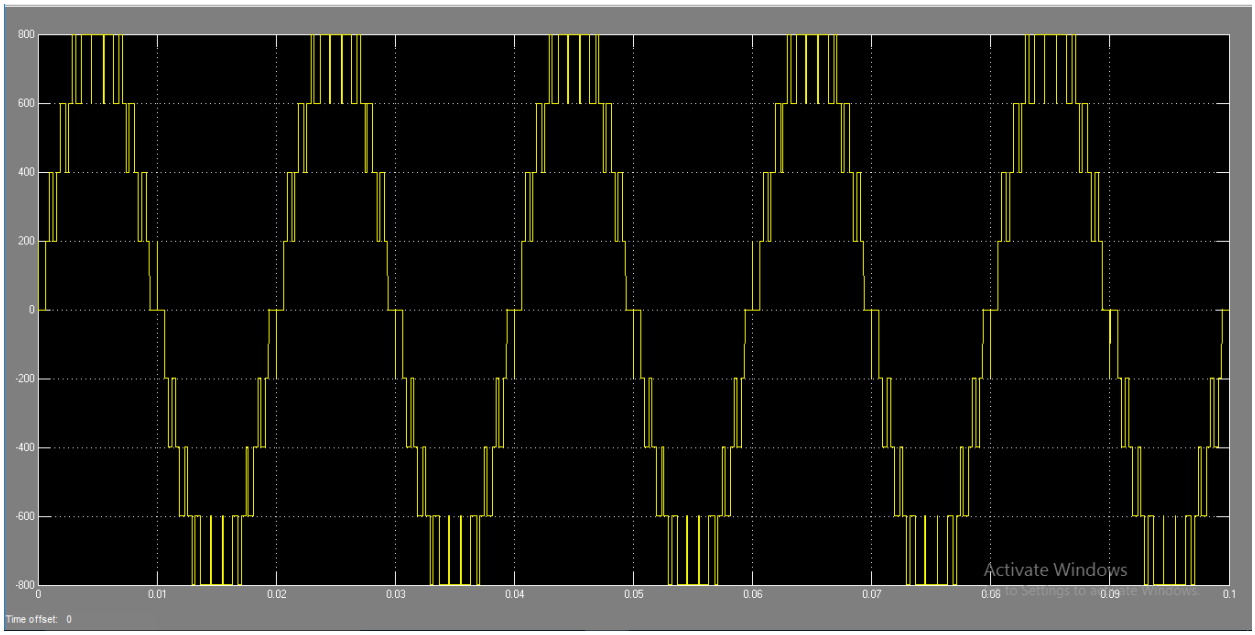


Fig.7: VOLTAGE WAVEFORM FOR 9 LEVEL CHBMLI

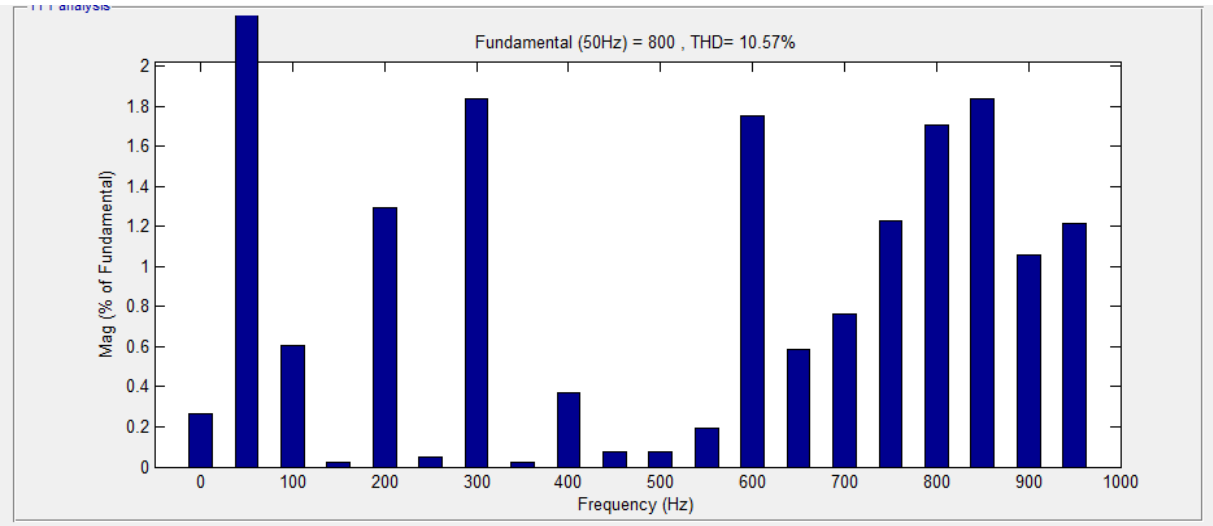


Fig.8: THD FOR 9 LEVEL CHBMLI

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4. **9-level switched capacitor based multilevel inverter**

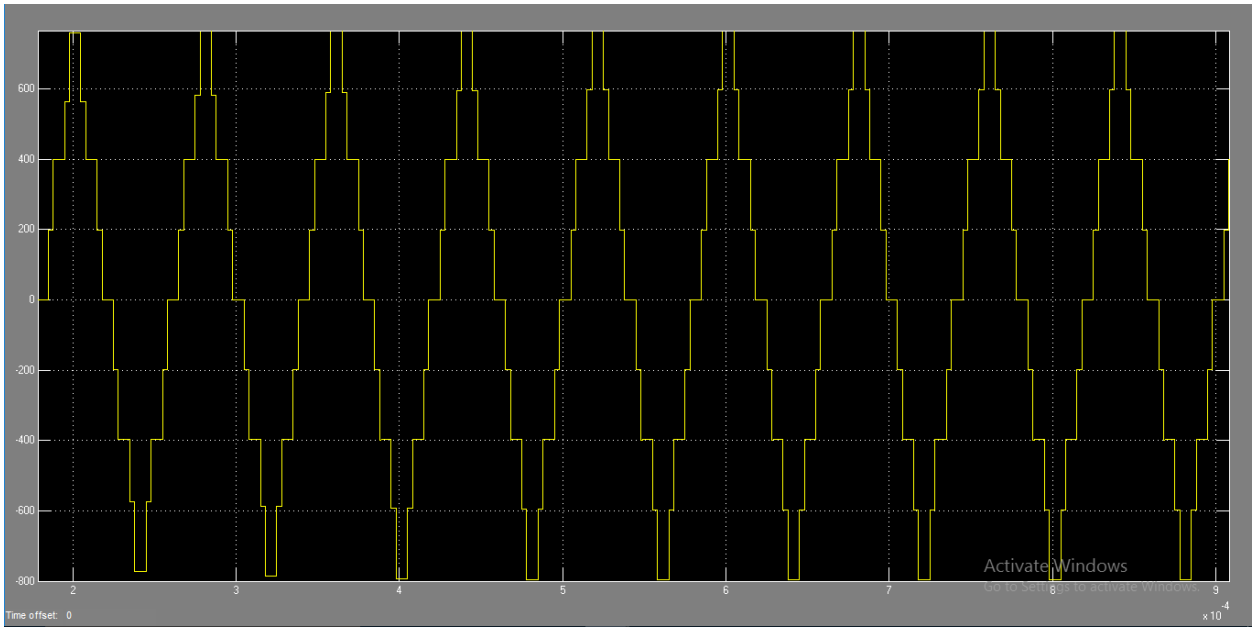


Fig.9: OUTPUT WAVEFORM FOR 9 LEVEL SCMLI

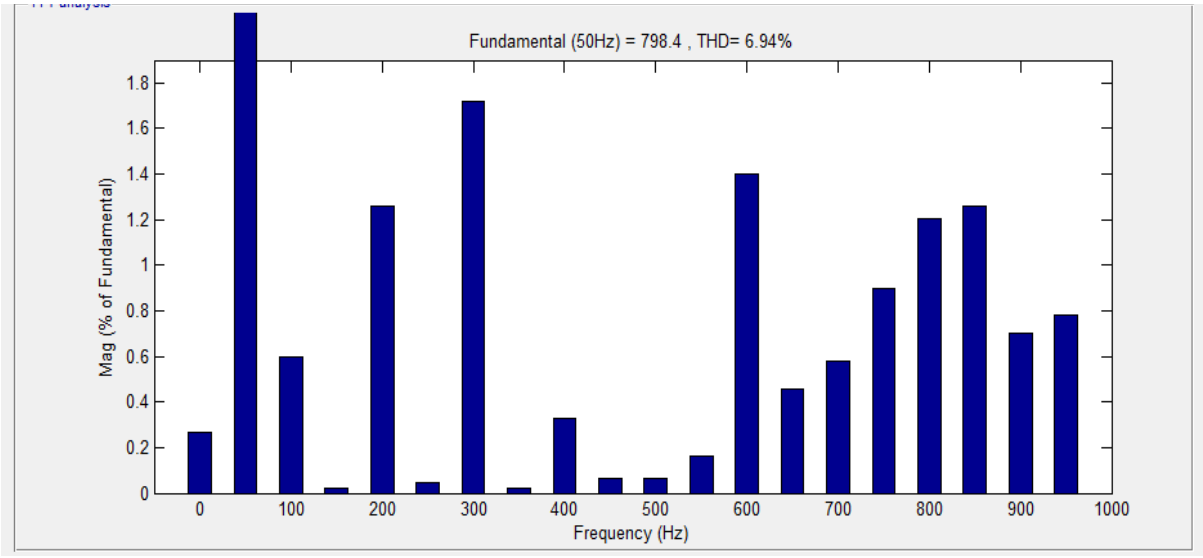


Fig.10: THD FOR 9 LEVEL SCMLI

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- **COMPARISON:**

| INBUILT | Switched capacitor based 9-level MLI | 9-level CHBMLI |
|---|---|---|
| No of DC source | 2 | 4 |
| No of switches | 12 | 16 |
| No of level in output | 9 | 9 |
| No of gate drivers | 12 | 16 |
| No of capacitor | 2 | 0 |
| No of diodes | 2 | 0 |
| THD | 10.12% | 10.57% |

**CONCLUSION:**

The proposed SC MLI is compared with conventional topology on the basis of no. of dc sources, no. of switches, no. of discrete diodes, no. of levels in output, no. of capacitors, no. of gate drivers is done and find that proposed topology is better in every domain with better harmonic distortion percentage.

Phase shifted modulation technique is used to modulate the gate pulses of 9-level inverters and there simulation is developed in MATLAB platform. From the obtained results by simulations it is observed that level shifted technique can be useful to multilevel inverter.

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