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# POWER EFFICIENT DESIGN OF ADIABATIC APPROACH FOR LOW POWER VLSI CIRCUIT

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**ABSTRACT**
In the current situation, low power VLSI circuits are produced by minimising power consumption in electronic circuits via the use of the adiabatic technique. For low power consumption, adiabatic logic circuits come in a variety of forms. This article proposes a comparison of the power consumption of adiabatic logic utilising Positive Feedback Adiabatic Logic (PFAL) and Two Phase Adiabatic Static Clocked logic (2PASCL). Flip flops are the primary parts in digital design that are in charge of storing in every SOC. Using both adiabatic topologies, the power consumption of the D-Flip flop and T-Flip flop is compared. Tanner EDA findings were used to create complete adder T-Flip flops in both topologies. The result demonstrates that a T-Flip flip that uses 2PASCL is more power-efficient than one that uses PFAL. This study presents the design of a 2-bit binary Magnitude Comparator (MC). Pass transistor logic (PTL), a kind of conventional CMOS (CCMOS) logic, was used in the design of the proposed MC. To perform assessment and comparison, the design is simulated alongside five other extant MC concepts. The suggested 2-bit MC showed a respectable degree of power and performance increase. Because of this, a considerable improvement in the Power Delay Product (PDP) may have been achieved. Owing to the notable improvement in performance, the suggested MC may be regarded as a very successful substitute for the current MC designs.

## 1. INTRODUCTION

### 1.1 OBJECTIVES

An increase in the level of integration in modern Very Large Scale Integration (VLSI) technology has rendered possible integration of many complex components in a single chip. Moreover, an analog circuit techniques in the front end wireless communication demand for a digital domain to save power. In most of these applications, multipliers have been an obligatory component and determine overall circuit performance with respect to speed, power consumption and size. Hence, the goal of this research work is formulated to design an comparator with less delay, low power consumption and compact area. In general, the performance of comparator in terms of delay, power consumption and area can be improved by two methods.

First one is based on efficient implementation of comparator function, whereas, another relies on proper selection of logic style for its implementation. There has been various multiplication methods for realizing the low power and high speed comparator introduced in the last few decades. However, in these multiplication techniques, the intermediate computation involved in the comparator operation reduces the speed exponentially in accordance with the width of the comparator input bit. This becomes a critical issue for a higher number of input bits. But this issue can be mitigated by the addition of partial products in parallel, which is adopted from mathematics based multiplication. Hence, this 2 work explores possible techniques on an existing

 

comparator for the better performance. As stated earlier, the logic styles used for realizing the multipliers have significant influence on the speed, size, power consumption and wiring complexity. Numerous logic styles in the classes of static Complementary Metal Oxide Semiconductor (CMOS), dynamic, transmission gate, Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) logic are discussed in the literature. Among them, GDI is considered in this research work due to its merits of low power consumption and implementation of any functions with low transistor count. However, the gates based on this logic are suffered from a low output voltage due to the threshold voltage drop. This has motivated us to propose an improved set of gates that operate with merits of full swing without increasing the fabrication complexity with the possibility of implementing with less transistor count.

Based on these gates and adders in mind, new compressors and parallel adders shall be designed. Further, the comparator shall also be realized with the help of these designs.

The objectives of the research work are listed as follows:

- To propose the gates namely, AND, OR, XOR and XNOR with full swing GDI logic and to extend the designed gates for implementing the full comparator designs.
- To improve the performance of parallel adders by implementing them using aforementioned full swing GDI gates and comparator
- To propose comparator architecture with less delay, low power consumption and small area using the concepts with full swing GDI logic

## 1.2 Problem specification

The logic styles used for realizing any digital design has a direct influence the speed, size, power consumption and wiring complexity. Different logic styles tend to favor the accomplishment of one performance aspect at the expense of others. These logic styles are varied in respect to the method of computing intermediate nodes, the number of transistor count though they are implementing the same function. Numerous logic styles in the classes of static CMOS, dynamic, transmission gate, GDI logic and Pass Transistor Logic (PTL) are discussed. The problems in the existing design styles as follows

- CMOS is the most common design technique, where each logic network will have pull up and pull down devices which are controlled by gate input signals. The merit of CMOS circuit is that the static power dissipation is very small and produces minimal leakage. However, the power dissipation of a CMOS device depends on its operating frequency. Whenever the frequency of input signal increases, the CMOS devices dissipate more power. As the input capacitances of a CMOS gate get larger, its propagation delay is higher compared to other logic styles.
- PTL circuits implement a logic function as a network of MOS transistors. They are well suited for pipelined circuits and have enhanced performance over conventional CMOS circuits in terms of silicon area, speed and reduced power dissipation. However, this logic has the drawback of reduced output voltage drop. This problem can be overcome by the use of swing restoration buffer at the output and this logic style is named as Complementary Pass transistor Logic (CPL).
- Usually, a CPL gate consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals. Because

 

the MOS networks are connected to variable gate inputs rather than constant power lines, only one signal path through each network must be active at a time, in order to avoid shorting different inputs together. The CPL gates have small input loads and good output driving capability due to the output inverters and the fast differential stage due to the cross-coupled PMOS pull-up transistors. This attributes to CPL's high speed. CPL is mainly used to implement complex functions (XOR and MUX) which employ smaller and fewer transistors.

- With the absence of the pull-up PMOS transistors, the output voltage swing of CPL gate is lower than the input swing by the NMOS threshold voltage, because CPL gate is constructed from NMOS transistors only. If the CPL output is used to drive an inverter, DC current may flow in the output inverter because the PMOS transistor of the inverter is not completely OFF. This is eliminated by adding the pull-up PMOS transistors. In CPL the Boolean function is evaluated using CPL network and full swing output is achieved using static CMOS inverter. But the problem incurred with this configuration is leakage current through static inverters. Furthermore, the layout of CPL cells is not as straightforward and efficient as CMOS, due to its irregular transistor arrangements and high density wiring.
- As an alternate to CPL, Swing Restored Pass transistor Logic (SRPL) has been used which consists of two parts namely, a complimentary output PTL network and a swing restoring circuit. The former is constructed with NMOS devices and the latter is constructed with cross coupled CMOS inverters. The inputs in SRPL technique are connected to drain and gate of PTL network. Here the pass variables are connected to the drain of the logic network transistors and the control variables are connected to the gates of the transistors. This type of arrangement nullifies the shortfalls associated with PTL and CPL. Nevertheless, in SRPL when proper device scaling is not provided then discharging the output for '1'-'0' transition becomes a bottleneck and consequently, the output degrades.

- Another widely used logic style is dynamic, which helps to implement large number of applications such as high speed digital logic. This logic family offers a number of interesting features compared to static logic, namely reduced transistor count (almost half compared to static CMOS) as well as reduced load capacitance and hence improved speed. An operation in a dynamic logic gate is controlled by a clock signal and can be implemented in either Pull-up (PMOS) or Pull-down (NMOS) configurations. The voltage at the output of the dynamic circuit is stored on a parasitic capacitance, which is typically buffered before it is sent to the next stage. This temporary voltage is affected not only by charge sharing of the internal parasitic capacitances but also by the consequent dynamic circuit.
- GDI logic has been introduced as an alternative to CMOS. It is a low power design technique which helps to realize the logic function with lesser number of transistors. Using this logic style, design of various arithmetic and logic circuits are developed.

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## 1.3 Methodologies

While the growth of electronics market has driven the VLSI industry towards very high integration density and system on chip, critical concerns have been arising on a severe increase in power consumption and area. High power consumption raises temperature profile of the chip and affects overall performance of the system. Moreover, the explosive growth in laptops and portable personal communication systems demand long battery life at the modest performance. This necessitates an intensive research in low power and low area integrated circuit design.

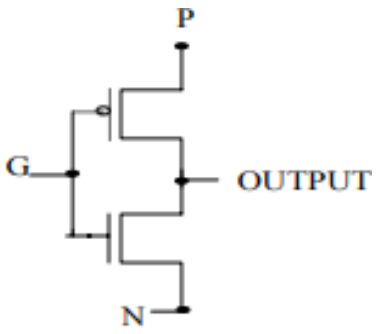


Figure 1.1 Basic GDI cell

GDI logic is introduced as an alternative to CMOS logic. It is a low power design technique which offers the implementation of the logic function with fewer numbers of transistors. The basic GDI cell is shown in Figure 1.1.

Though it resembles a conventional CMOS inverter, the source and drain diffusion input of both PMOS and NMOS transistor is different.

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On one hand, in conventional inverter circuit, source and drain diffusion input of PMOS and NMOS transistors are always tied at VDD and GND potential, respectively. On the other hand, the diffusion terminal acts as an external input in the GDI cell. The realization of various Boolean functions such as F1, F2, OR, AND, MUX and NOT are listed in Table 1.1

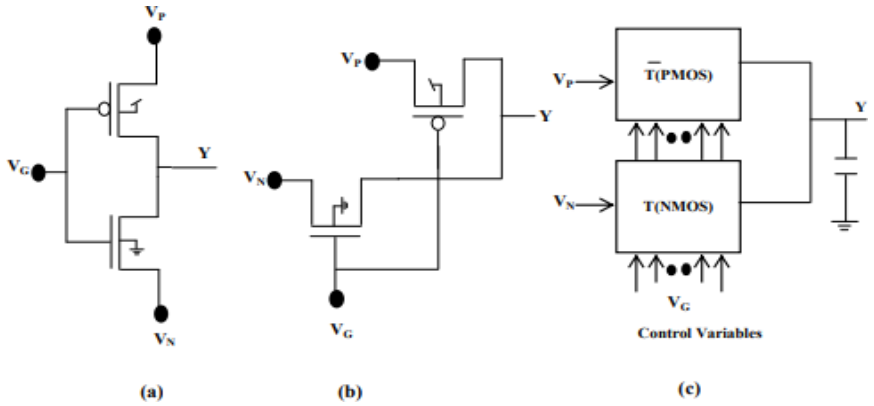


Figure 1.2 (a) Basic GDI cell using inverter structure (b) alternate basic GDI cell representation using PTL (c) General block diagram of GDI logic

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A Gate Diffusion Input (GDI) technique inherits the properties of PTL and CMOS. The basic structure realization resembles the CMOS inverter and the operational feature resembles the PTL logic. GDI basic cell and general block diagram is depicted in Figure 1.2. The basic cell structure realization is similar to CMOS inverter containing series connected PMOS and NMOS. Each GDI cell contains three inputs: VG is the shorted gate input common to PMOS and NMOS, VP is the drain/source P-diffusion input at the PMOS terminal and VN is the source/drain N-diffusion input at the NMOS terminal. Any Boolean function in GDI technique where simple or complex is realized using this basic structure. A basic GDI cell is a multiplexor circuit with gate control variable and diffusion inputs.

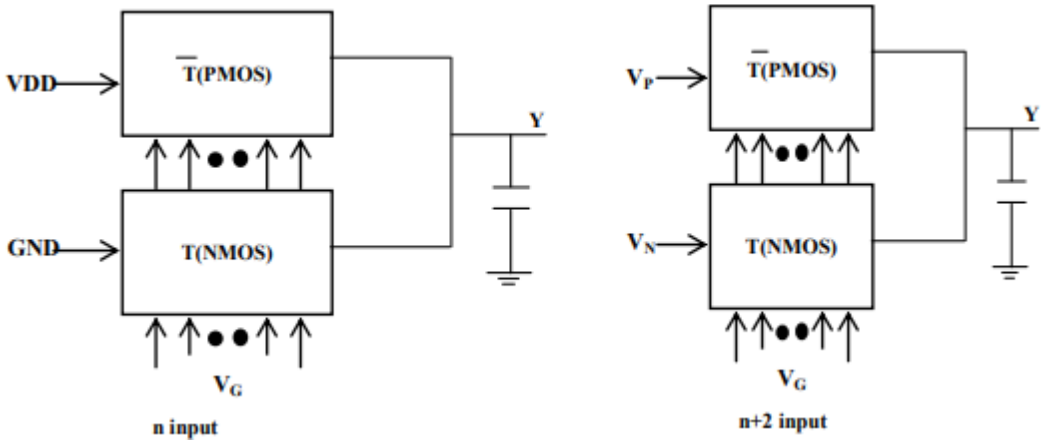


Figure 1.3 (a) Fan-in of CMOS structure (b) Fan-in of GDI structure

So in general the fan-in specifications of GDI are defined as (n+2) in terms of CMOS logic, where n defines the number of inputs. The fan-in requirements of GDI and CMOS are shown in Figure 1.3. Due to high fan-in features more number of logic can be accommodated with minimum number of transistors which improves the overall performance of the complex systems but the only restrictions are the body effect considerations.

### 1.3.1 OPERATIONAL CHARACTERISTICS

Fundamentally the basic GDI cell is a pair of 2-to-1 multiplexer where the functionality of the cell is defined by the control signal connected to the gate terminal VG. If the control input is low the output of the multiplexer is driven by the P-diffusion input. On the other hand for the control input being high produces the multiplexer output to be driven by the N-diffusion input. To illustrate the operational characteristics of this basic GDI cell, consider the case when the control input at terminal VG is low, P-diffusion input VP is high and N-diffusion input VN is low, which makes the PMOS device to enter into linear region and the device is set to be in ON state, while NMOS enters into cut-off region and the device is OFF which produces direct path between VP and output. Consequently the output of the multiplexer will be high. The operational features of the basic GDI cell in Figure 1.1 with various input combination along with the PMOS and NMOS device characteristics are listed in Table 1.2.

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Table 1.2 Operational characteristics of basic GDI cell

| Input $V_G$ | Input $V_N$ | Input $V_P$ | PMOS device characteristics | NMOS device characteristics | Output y |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Linear: $V_P-V_{TP}<Vout<V_{DD}$ | Cut-off: $V_N<V_{TN}$ | Bad 0 |
| 0 | 0 | 1 | Linear: $V_P-V_{TP}<Vout<V_{DD}$ | Cut-off: $V_N<V_{TN}$ | Good 1 |
| 0 | 1 | 0 | Linear: $V_P-V_{TP}<Vout<V_{DD}$ | Cut-off: $V_N<V_{TN}$ | Bad 0 |
| 0 | 1 | 1 | Linear: $V_P-V_{TP}<Vout<V_{DD}$ | Cut-off: $V_N<V_{TN}$ | Good 1 |
| 1 | 0 | 0 | Cut-off: $V_p>V_{DD}+V_{TP}$ | Linear:$0<Vout<V_N-V_{TN}$ | Good 0 |
| 1 | 0 | 1 | Cut-off: $V_p>V_{DD}+V_{TP}$ | Linear:$0<Vout<V_N-V_{TN}$ | Good 0 |
| 1 | 1 | 0 | Cut-off: $V_p>V_{DD}+V_{TP}$ | Linear:$0<Vout<V_N-V_{TN}$ | Bad 1 |
| 1 | 1 | 1 | Cut-off: $V_p>V_{DD}+V_{TP}$ | Linear:$0<Vout<V_N-V_{TN}$ | Bad 1 |

It is noticed for the inputs (0,0,0) and (0,1,0) the output is worsened due to the threshold variation of PMOS and the output is polarized owing to the formation of reversible diodes between PMOS and bulk terminal at the output side. Similarly for the inputs (1, 1,0) and (1,1,1) the output is degraded due to the threshold variation of NMOS and the formation of diodes between NMOS and bulk resulting in static power dissipation and the output is approximately equal to VDD-VTN. The switching activity of GDI cell is portrayed in Figure 1.4.

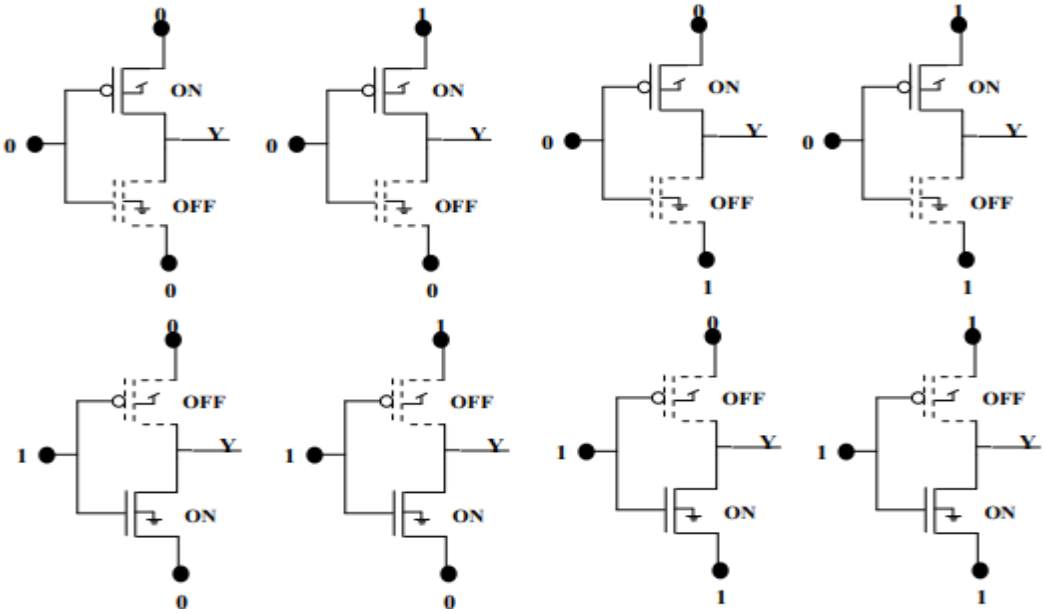


Figure 1.4 Switching activity of GDI cell

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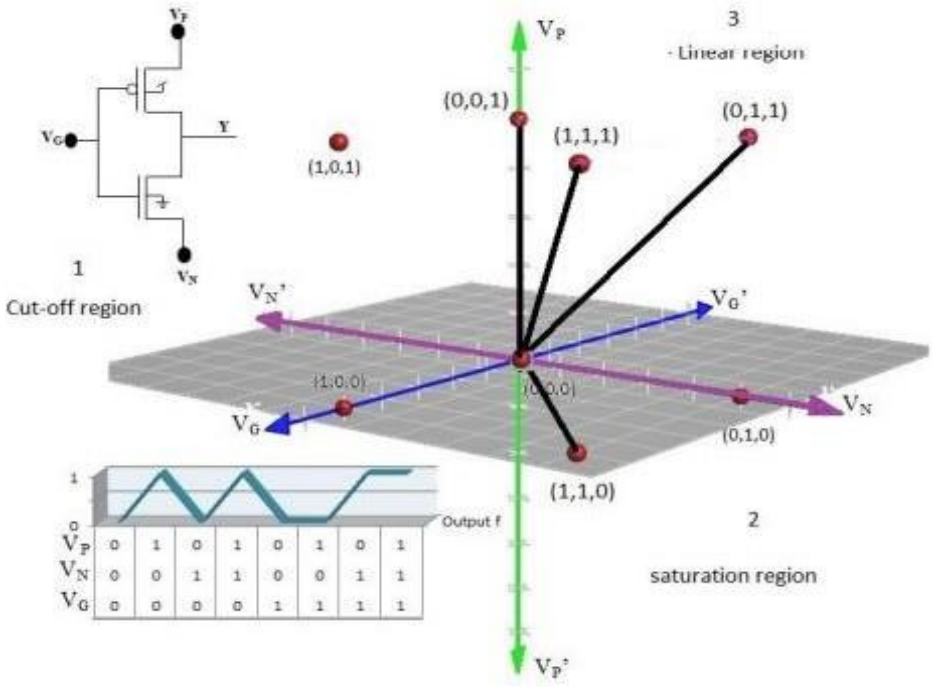


Figure 1.5 3-D operational characteristics of basic GDI cell

## 1.4 Contributions

The circuit realization of low power and low area has become an important issue due to the increasing demand for mobile electronic devices such as cellular phones, laptop and so on. The ALUs and digital gates act as building components in DSP architectures and microprocessors. Therefore, their design of them with low power, smaller area and faster speed is in great demand. Standard implementations with various logic styles have been used in the past to design gates and full comparator cells. The logic styles used in the design basically influence the speed, size, power consumption and wiring complexity of the circuit. The GDI logic is considered in this thesis due to its merits of low power consumption and requirement of less transistor count than other logic styles, subsequently resulting in smaller area.

- In this work, the design of gates namely, AND, OR, XOR and XNOR will be designed. In addition, with the help of these gates three designs of full comparator are implemented with the merits of low power consumption, less delay and small layout area.
- Parallel adders are developed to minimize the delay involved in the binary addition task and are well suited for VLSI implementation. The performance of these adders can be greatly influenced by the performance of their basic modules. In this work, an efficient implementation of parallel adders using GDI logic is developed.

## 2. LITERATURE SURVEY

An extensive literature survey is carried out in order to confirm the need for the proposed objective. Initially, the reason for selection of GDI logic and its bottlenecks are explained, and then the full swing mechanisms available in the literature for GDI logic are discussed. Further, the earlier works on arithmetic circuits namely, full comparator and compressor are explained.

 

In addition, the existing implementations of parallel adders and the necessary improvements on their architecture are given. Also, the existing works relating comparator are discussed. Finally, the existing hierarchy multiplier architecture and its associated drawbacks are discussed.

**2.1 Survey of Literature**

In [1] authors proposed a reduction of delay, leakage current, leakage power. First find out the leakage current and leakage power. Which uses a gate diffusion input technique. By using this no of transistor is reduced. If number of transistor is reduced, area is also reduced, leakage current also affected. To study all parameter in this thesis uses a 2x1 MUX, 4x1MUX,16x1 MUX and comparator. Applying a GDI technique and also implemented by using a CMOS technique. Then do comparisons on GDI and CMOS technique and do a capacitance calculation. To implement all those things use a microwind 3.1 and DSCH 2.0. It is an Electronic Design Automation (EDA) environment that allows implementing a integrating in a single framework different applications and tools, allowing supporting all the stages of IC design and verification from a single environment. The resulting layout must verify some geometric rules dependent on the technology (design rules). Now checked with a Design Rule Checker (DRC) to find any error in the layout diagram and them simulation is performed. In implementing and do a comparisons of GDI and CMOS technique.

In [2] authors proposed the comparator is a one of the most basic operational unit in any processor. The comparator can be defined as the combinational unit which is used to perform its logical and arithmetic units. This paper presents a low power high speed comparator(comparator) in 14 nm technology using Multi-threshold voltage transistor logic and Gate Diffusion Input technique. Its performance is compared with conventional CMOS technique. The simulated results revealed better performance characteristics of various arithmetic and logic functions of a 1-bit comparator using MTV and GDI techniques compared to conventional CMOS technique. This technique allows reducing power dissipation and delay while maintaining low complexity of logic design.

## 3. PROBLEM DEFINATION

Low-power design has become a critical issue in Very Large Scale Integration (VLSI) design, especially for portable devices and high-density systems such as lap top, desk top and mobile phones. For submicron Complementary Metal Oxide Semiconductor (CMOS) technology; area, topology selection, power dissipation and speed are the imperative aspects. In the contemporary VLSI systems power dissipation is exceptionally high due to the sudden switching activity of internal signals. Several monumental changes have occurred in the development of electronic circuits by scaling the component size to accommodate millions of transistors in a single chip. This miniaturization increases the complexity of VLSI circuits in terms of power consumption and speed. According to Moore [Moore's law, 1965] the number of fabricated transistors in a single Integrated Circuit (IC) doubles every two years, which calls for higher consumption of power which in contemporary times becomes a challenge and a critical factor. Therefore power reduction has become a critical concern in today's hardware implementation process.

The energy dissipation theory propounded by Landauer [Landauer, 1961] states that at least KTln2 joules [where K =1.3806*10-23m 2 kg-2K -1 (joule/kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed] of energy is dissipated by a system for every single bit of operation. Generally the heat dissipated due to the loss of single bit of information will be comparatively

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petite at room temperature. However if the number of bits is increased the heat dissipation becomes predominant which affects the performance of the device leading to reduced life span of the system. Therefore reduced power consumption in the wake of increased operation becomes a logical corollary. Towards this objective, optimizations are required at various levels of the design steps, such as the algorithm, architecture, logic, circuit and process technology.

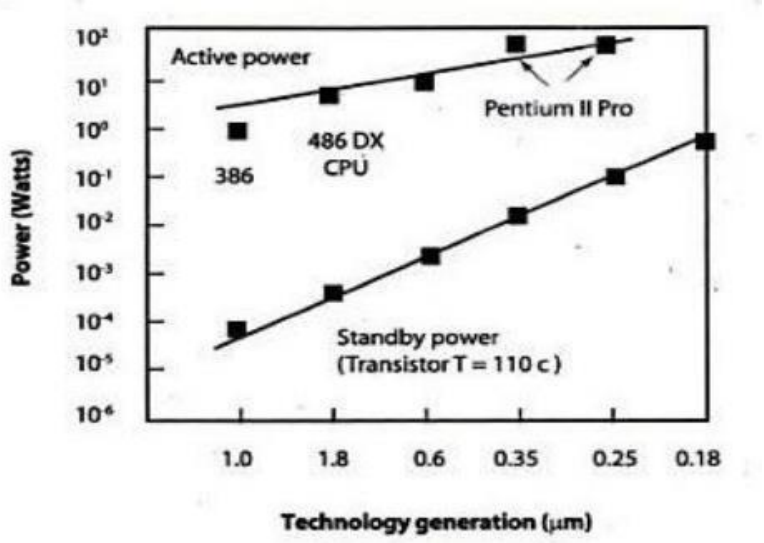


Figure 3.1 Short circuit power evolutions with respect to technology

The challenge of power reductions is addressed by several multifaceted optimization approaches such as the technology used for the construction of design, the logic topologies, the circuits, architectures and algorithm.

The aim of this research work has been achieved through dual goals in order to improve the performance of comparator in terms of delay, power, Power-Delay Product (PDP), transistor count and operating frequency. The former goal defines the creation of synthesizable library along with power-delay model and the latter goal defines the creation of fundamental components using the proposed EGDI library. Therefore, the specific goals are:

- To enhance the Gate Diffusion Input (GDI) Technique in order to improve power dissipation and speed of logic design and to develop the synthesizable library along with delay-power model for normal and skewed gates.
- To study current comparator processor architecture and technology implementation.
- To modify the Gate Diffusion Input (GDI) Technique and to propose an Enhanced GDI Technique for power-speed efficient design using unified method of signal arrangement.
- To develop a synthesizable library for circuit realization in Enhanced GDI Technique.
- To develop the Mathematical Models for delay and power characteristics for the synthesizable library for normal and skewed gates.
- To implement the functional core for comparator unit

## 4. PROPOSED METHOD

In today's VLSI technology, power consumption plays vital role. Adiabatic approach offers the best way to use the energy stored in load

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capacitors instead of discharging to the ground. It originates from the word "thermodynamics" which means no energy dissipation [2].During the past decades CMOS was responsible for creating low power equipment. Power consumption is mainly caused due to the load capacitors switching activity. The two major types of dissipation are static and dynamic [4].The switching activity of load capacitor causes the dynamic dissipation. When the circuit is not in working condition, internal leakage is caused in devices which constitutes the static dissipation. Dynamic dissipation plays an important role in circuits [7].Power dissipation in CMOS can be reduced by decreasing the terminal capacitance value and by reducing the voltage supply. This results in low performance of device. Hence an efficient model is proposed for low power consumption and low power dissipation which is termed as adiabatic logic circuits. In this method the energy is regained by sending back to power supply thereby reducing the entire power consumption .Full adder blocks plays a very important role in adder design. In this paper the performance of adiabatic style of two phase adiabatic static clocked Logic (2PASCL) and Positive Feedback adiabatic logic (PFAL) is evaluated and the simulation results shows which is the best approach for the design of flip flops.

**ADIABATIC LOGIC**

The present day portable devices need enormous amount of energy backup. Energy efficiency is the main concern in today's circuits. This is achieved by the low power consumption and low power dissipation of the circuits. Charge recovery principle is used in the adiabatic logic circuits. The energy is not dissipated but it is recycled. The energy stored in load capacitor is given by [3]. E stored= 1/2 CLVdd2 (1) The amount of energy wasted during the discharge of the load capacitor is given by "(1)".CMOS played a very important role in power reduction. But later an efficient method was designed to overcome the disadvantage of CMOS. Adiabatic approach used, consumes less power and has low power dissipation. It recovers the energy that is wasted in CMOS circuit. There are two types of adiabatic logic [5].They are Partial and Full adiabatic logic. The 2PASCL and PFAL comes under Partial adiabatic category.

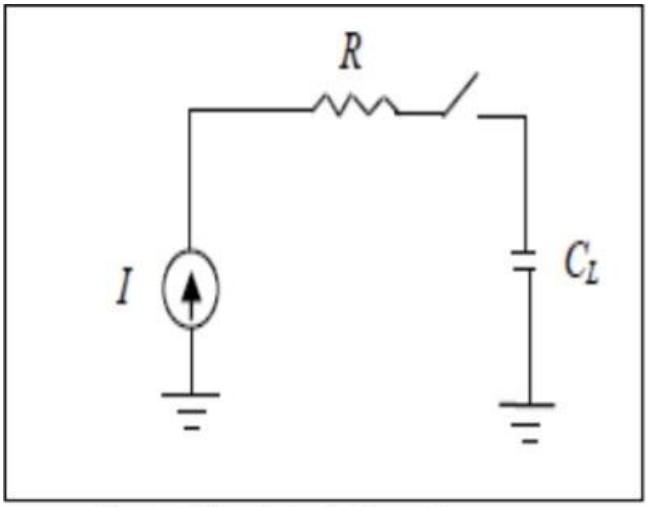


Fig. 1. Adiabatic Logic Circuit [2]

A. Positive Feedback Adiabatic Logic(PFAL)

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It was introduced by Vetali in 1996 which consist of 2 NMOS transistors and 2 PMOS transistors. It is formed by cross coupled PMOS pair. The circuit is represented in Fig 2 and the corresponding four phases are drawn. It consist of two inverters which are cross coupled. There are four phases in adiabatic logic circuits .They are 1. Evaluation Phase 2. Hold Phase 3. Recovery Phase 4. Wait Phase During the wait phase the power clock is at low state and the value is zero .During evaluation phase, the power supply increases to Vdd from zero. In the hold phase, the power clock remains high which provides constant input to the preceding stage. The power supply decreases to zero in the recovery phase. The power source recovers all the energy back which is the principle of adiabatic logic.

B. Two Phase Adiabatic Static Clocked Logic(2PASCL)

There are two MOSFET diodes. One is near the pull up network and the other one is in the pull down circuit [6].The 2PASCL works in two phases. One is Evaluation and the other is Hold phase [1]. During the Evaluation phase when the input is at logic zero, the PMOS is ON and the NMOS is OFF. The capacitor charges and the output is zero and it discharges through NMOS. The energy is sent back to the power supply at the pull up network

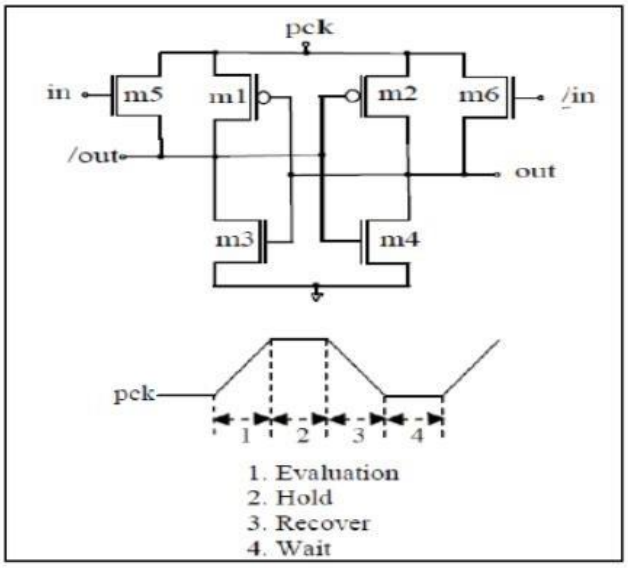


Fig. 2. PFAL Logic Circuit

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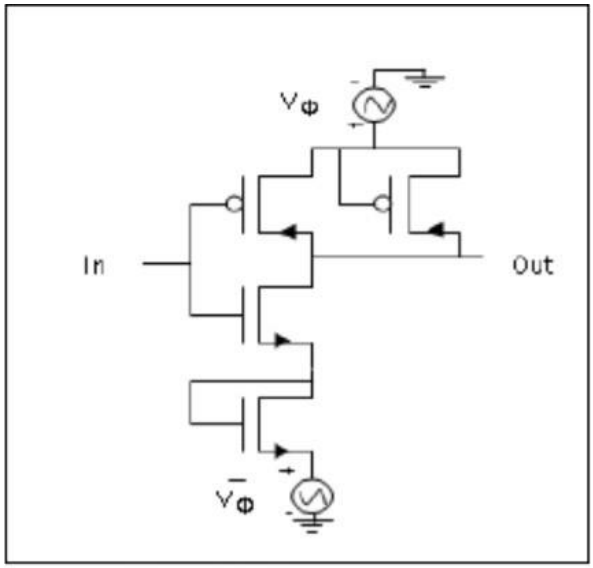


Fig. 3. 2PASCL Logic Circuit

OFF. The capacitor charges and the output is zero and it discharges through the PMOS. The energy is sent back to the power supply at the pull down network. The switching activity is reduced due to the use of sinusoidal AC power supply in 2PASCL thereby reducing the power dissipation.

**PROPOSED DESIGN**

A. D-Flip Flop using 2PASCL

The circuit proposed is the D flip flop using 2PASCL adiabatic logic and it is designed using Tanner EDA tool which is shown in Fig 4.

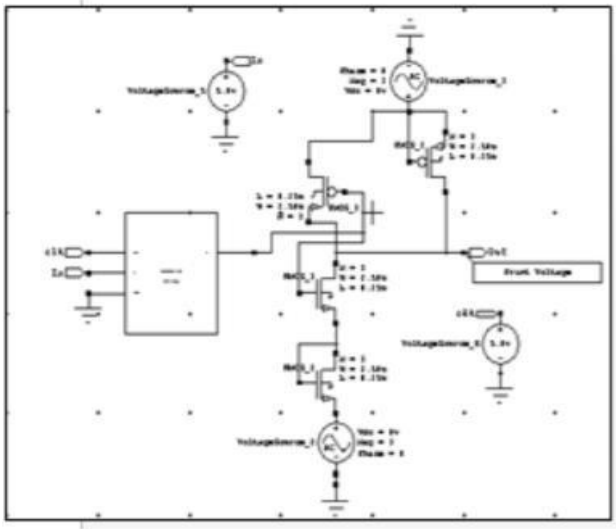

Fig. 4. Schematic of D-Flip flop using 2PASCL

## 5. EXTENSION METHOD

The evaluation of modern highly complicated electronic circuits and devices have led to the invention of several smart systems [1-5]. These smart systems require highly effective VLSI circuits which have high computation speed at a satisfactory level of power loss [6-8]. Performance of VLSI circuits plays important role in portable devices because of the requirement of low power dissipation with

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acceptable speed. Moreover, the modern microprocessors require highly efficient circuits with limited area consumption to maintain their high functionality and high integration density. Therefore, design methodologies in VLSI circuits have gained a tremendous amount of interest in the research community. MC deign in VLSI circuits is an arithmetic component that can decide if a binary number is equal, greater or less than a another given binary number [9]. In short, MC is used for binary number comparison [10]. Generally, MC takes two binary numbers as inputs and provides the binary comparison results as outputs. MC is massively used in instruction sorting in microprocessors [11]. Digital signal and parallel processing operations requires efficient MC circuits to maintain high performance [12-13]. Hence, due to the application of MC in high performance systems, using optimal MC design is highly necessary. Binary MC is an elementary level of operation in digital VLSI circuits and systems. Binary 2-bit MC is considered as basic block for implementation of wide word bit MCs. Therefore, the efficient design of a 2-bit MC can bring about massive changes in the performance. Therefore, in order to build an efficient MC block, optimal design of 2-bit MC plays quite significant role.

**Schematic of porposed 2-bit MC:**

Full schematic of the proposed 2-bit MC is shown in Fig. 3. The XNOR gates are implemented as per described in the previous sub-section. For, AEB, CCMOS logic is used although it requires high transistor count. The reason for using CCMOS AND gate for AEB is this AND gate provides output signal for which high drive power is required. ALB and AGB are implemented using complex logic network implemented in CCMOS logic using the equations (2)-(3). The transistor counted from Fig. 3 is 46. Hence, the proposed 2-bit MC design needs only 46 transistors to fully implement its operation.

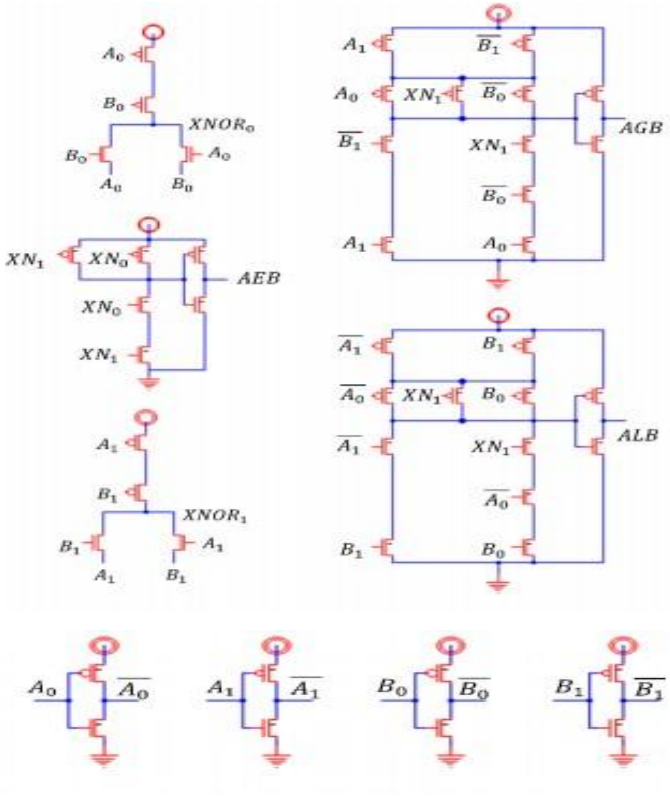


Fig. 3. Proposed 2-bit MC

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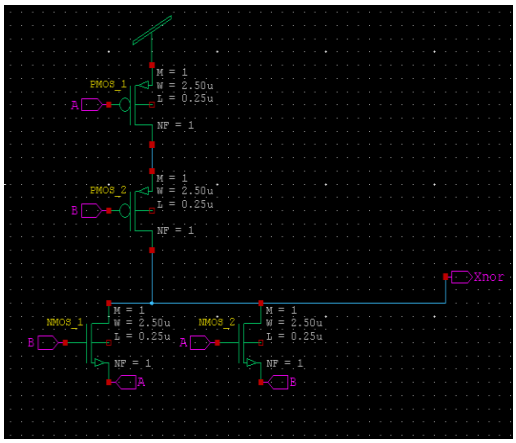
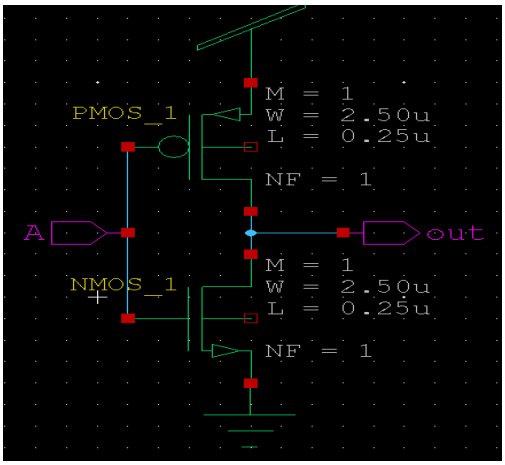
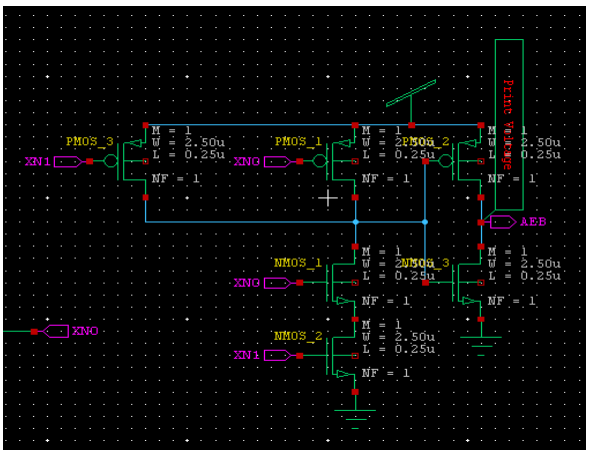
## 6. SIMULATION RESULTS



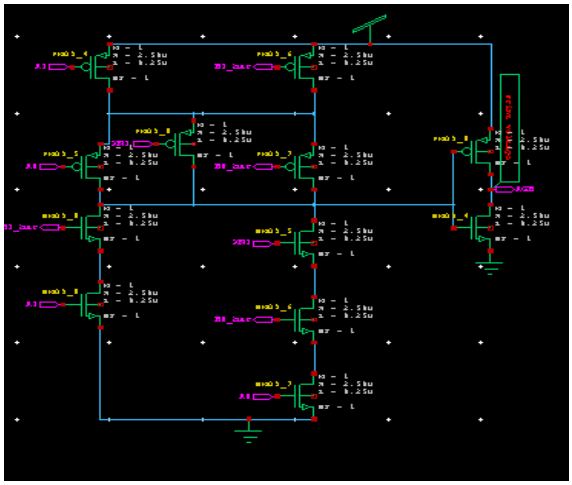

**XNOR**



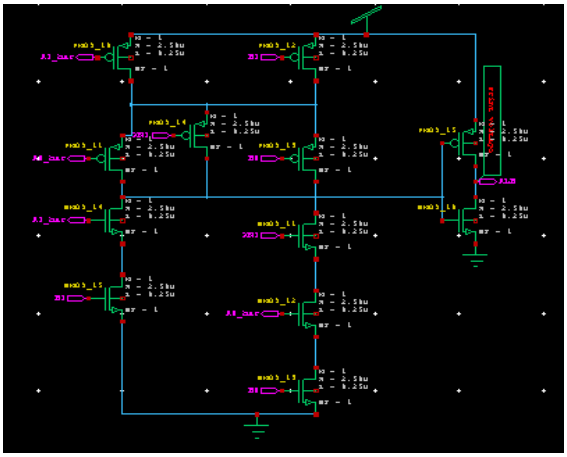

**NOT**



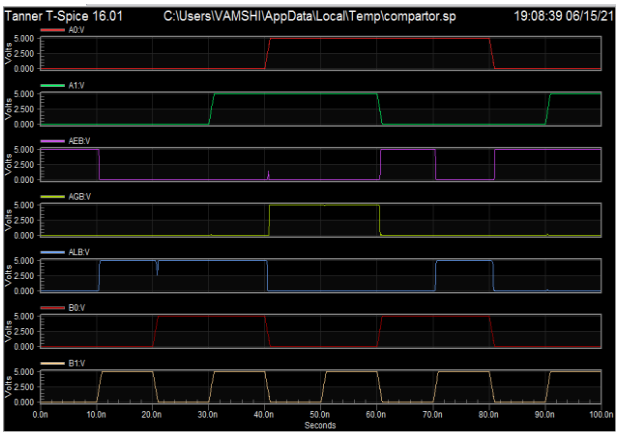

**A equal B**



**A greater than B**



**A less than B**




**Simulation**

Device and node counts:
MOSFETs - 46
MOSFET geometries - 2

Voltage sources - 5
Subcircuits - 6
Model Definitions - 2

Computed Models - 2
Independent nodes - 69
Boundary nodes - 6
Total nodes - 75
*** 6 WARNING MESSAGES GENERATED DURING SETUP
Warning : Newton solver has failed due to extremely large node voltages.
: If the circuit has very high gain and extremely large voltages (>1000V) are expected,
: then you may use '.option vmax=0' to disable this check.
Conventional DC operating point computation failed.
Gmin stepping succeeded
Final gmin value = 1e-012, dcstep = 0
Power Results
VVoltageSource_2 from time 0 to 1e-007
Average power consumed -> 7.763914e-007 watts
Max power 1.715898e-003 at time 4.07997e-008
Min power 0.000000e+000 at time 0
Parsing 0.06 seconds
Setup 0.08 seconds
DC operating point 0.50 seconds
Transient Analysis 0.86 seconds
Overhead 0.71 seconds
---
Total 2.21 seconds

## 7. CONCLUSIONS & FUTURE ENHANCEMENTS

### Conclusion

This study presents a 2-bit MC design using PTL and CCMOS technology. The design used complicated VLSI circuits based on CCMOS logic for the output signals and PTL technique-based VLSI circuits for the input terminals. To demonstrate the design's performance assessment, it is put into practice and contrasted with a number of other MC designs. The architecture demonstrated a significant improvement in PDP and latency while keeping power levels well below acceptable bounds. As an as a consequence, the suggested MC architecture is excellent for modern microprocessor design.

### Future works

The following recommendations are made in order to carry out the study: creating a CPU using the GDI technology, creating logic circuits using the GDI technique and nanotube carbon transistor, Create a multiplier using the GDI method. Digital integrated circuits have long been thought to have speed and power consumption goals, and in recent years, a great deal of research has been done in this field. Technology progress and chip size reduction have led to a notable rise in chip power density, or power per unit area. Reducing power consumption in digital integrated circuits is important since employing cooling on the chips is expensive. Chip density and speed have risen in tandem with the explosive growth of semiconductor device manufacturing technologies. One of the main concerns with portable devices is power consumption control. On these devices, high power usage shortens battery life. Even for non-portable devices, reducing power losses is crucial since rising losses drive up the cost of cooling and package density. Multiple VLSI chips are present in portable electronic gadgets because of their complicated structural design. Non-digital parts make up the majority of a portable electronic device's losses. Dynamic power management refers to efficient methods for lowering power losses in such systems that are associated with the removal or cessation of leakage components. Multiple dynamic power management strategies may be utilised in older systems; this may make integration challenging and necessitate repeating many projects as well as troubleshooting. IC power loss is composed of several elements and is contingent upon the kind of circuit performance.

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