

# AN EFFECTIVE USAGE OF DUAL CURRENT MIRROR BASED VOLTAGE LEVEL SHIFTER

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## Abstract

Voltage level shifters play a crucial role in modern integrated circuit design, facilitating seamless communication between digital blocks operating at different voltage domains. This abstract introduces a novel Voltage Level Shifter architecture featuring a Dual Current Mirror configuration. The proposed Voltage Level Shifter leverages the benefits of dual current mirrors to achieve high-performance voltage level shifting while minimizing power consumption and area overhead. By employing a dual-current mirror setup, the design ensures efficient and reliable signal propagation between distinct voltage domains, a critical requirement for mixed-signal and multi-voltage integrated circuits. This paper presents a comprehensive analysis of the design, including theoretical underpinnings, simulation results, and practical implementation considerations. The dual current mirror configuration not only enhances signal integrity but also minimizes voltage drop, ensuring minimal distortion during the level shifting process. Furthermore, the proposed Voltage Level Shifter demonstrates superior performance in terms of speed, power efficiency, and robustness, making it a compelling choice for a wide range of applications, from energy efficient IoT devices to high-performance computing systems. The presented design represents a significant advancement in voltage level shifting techniques, offering a versatile and efficient solution for today's diverse and demanding integrated circuit requirements.

Keywords: current mirror, IoT, Level shifting, mixed signal

## I. Introduction

In the ever-advancing field of integrated circuit (IC) design, voltage level shifting is a fundamental operation that allows for the harmonious coexistence of digital and analog components operating at different voltage domains. This pivotal function ensures that data and signals can be accurately exchanged between these distinct domains, enabling the seamless operation of complex systems [1]. In the realm of mixed-signal ICs, where analog and digital subsystems coexist and collaborate, voltage level shifting becomes particularly critical. This paper introduces an innovative approach to Voltage Level Shifting (VLS) by leveraging a Dual Current Mirror configuration to bridge the voltage gap[2]. Voltage level shifting is not merely a technical necessity but a linchpin that underpins the functionality of modern electronic devices. As we continue to witness the relentless evolution of electronics, from energy-efficient Internet of Things (IoT) devices to high-performance computing systems, the demands for more efficient, versatile, and reliable voltage level shifting techniques have grown substantially. This introduction serves as a prelude to the exploration

of a novel VLS method that promises to address these contemporary challenges and redefine the standards of voltage translation in integrated circuits[3-5].

The Imperative of Voltage Level Shifting, in the realm of digital circuits, logic gates and flip-flops operate with a binary voltage representation, where a low voltage level (typically denoted as '0') and a high voltage level (usually '1') are used to encode and process information. However, the voltages used in these digital circuits vary depending on the technology and design constraints. For instance, older technologies may employ higher voltage levels, such as 5 volts, while more modern technologies, like CMOS (Complementary Metal-Oxide-Semiconductor), operate at significantly lower voltages, often around 1.8 or 3.3 volts. This variance in voltage levels can pose a significant challenge when attempting to interface digital components that operate at different voltage domains[6]. The need for voltage level shifting arises when digital blocks, operating at different voltage domains, need to communicate, exchange data, or synchronize their actions. This is a common scenario in mixed-signal ICs, where analog sensor data is processed and converted into digital signals, or in multi-voltage domain designs, which seek to optimize power consumption by using different voltage levels for various functional blocks. Voltage level shifting is an indispensable process that ensures that digital signals can traverse these voltage boundaries unscathed. The overarching goal is to enable signal propagation while preserving the integrity of the data, minimizing power consumption, and ensuring that signal transitions occur with minimal distortion [7]. This is particularly critical in applications where data accuracy and timing precision are paramount.

Historically, various techniques have been employed to address the challenges posed by voltage level shifting. Some of the conventional methods include the use of level shifters based on pass transistors, voltage dividers, and buffer amplifiers. Each of these methods comes with its own set of advantages and limitations. These level shifters use pass transistors to connect different voltage domains, allowing signals to pass from one domain to another [8]. While they are simple and area-efficient, they suffer from voltage drop issues, resulting in signal distortion, especially in low-voltage environments. Voltage dividers, typically composed of resistors, can be employed to scale down voltages. While they are relatively simple, they are slow and suffer from power inefficiency due to the constant current flow through the resistors, even when no signal transition is occurring. Buffer amplifiers are used to boost and shift signals to higher voltage levels. They are effective in maintaining signal integrity but can consume significant power and occupy substantial areas[9-10].

While these traditional methods have served their purposes, they come with trade-offs that may not be ideal for modern IC design objectives. The quest for more efficient, versatile, and reliable voltage level shifting techniques has fueled innovation in this field. This work introduces a groundbreaking approach to voltage level shifting that takes advantage of a Dual Current Mirror configuration. Current mirrors, a fundamental building block in analog and mixed-signal IC design, are known for their ability to accurately replicate a current, making them suitable for various applications. In this work, we explore how a dual current mirror setup can revolutionize the landscape of voltage level shifting by addressing the limitations of existing methods while capitalizing on the strengths of current mirrors [11]. The core idea behind the Dual Current Mirror Voltage Level Shifter is to use the dual current mirror setup to bridge the voltage gap between two domains efficiently and with minimal signal distortion. By replicating the input current, the dual current mirror ensures that the output voltage

faithfully represents the input signal, regardless of the voltage domain differences. This innovative approach offers several key advantages like Signal Integrity, the dual current mirror configuration minimizes signal distortion, ensuring that the output signal accurately represents the input, even when voltage domains differ significantly. Low Power Consumption, by design, current mirrors are inherently power-efficient, making the dual current mirror level shifter an attractive choice for applications where power efficiency is paramount[12].

High-Speed Operation, the novel design allows for fast signal propagation, making it suitable for high-performance computing systems and other time-critical applications. Reduced Voltage Drop, the dual current mirror approach significantly reduces voltage drop, ensuring that signal transitions occur with minimal distortion. Robustness, the design is versatile and robust, making it suitable for a wide range of applications, from low-power IoT devices to high-performance digital systems.

In the subsequent sections of this work, we delve deeper into the theoretical underpinnings of the Dual Current Mirror Voltage Level Shifter, provide insights into its practical implementation, and offer a comprehensive evaluation of its performance in terms of signal integrity, power efficiency, and speed. This innovative design represents a significant advancement in the field of voltage level shifting and promises to address the evolving challenges of modern IC design in an increasingly diverse and voltage-fragmented landscape.

## II. Literature Review

Voltage Level Shifting Techniques in Integrated Circuit Design. Integrated circuits (ICs) are the backbone of modern electronics, and they often comprise a mix of digital and analog components, each operating at distinct voltage levels. To ensure seamless interaction and data exchange between these components, voltage level shifting techniques play a pivotal role. This literature review explores the importance of voltage level shifting in IC design[13], examines traditional methods, and highlights the significance of innovative approaches to meet the evolving demands of the industry[5]. The Significance of Voltage Level Shifting Voltage level shifting is the process of adapting signal voltage levels from one domain to another within an IC. It is vital in enabling digital and analog components to communicate effectively, ensuring data integrity, signal accuracy, and proper operation of the circuit. The need for voltage level shifting arises from the coexistence of various voltage standards and the drive for increased integration, power efficiency, and compatibility in modern electronics. Traditional Voltage Level Shifting Techniques Over time, several conventional techniques have been established to address voltage level shifting.

These level shifters employ pass transistors[6] to connect voltage domains, allowing signals to pass from one to another. While straightforward and space-efficient, they often suffer from voltage drop issues, leading to signal distortion. Voltage Dividers: Voltage dividers, composed of resistors, divide voltage levels. They are simple but relatively slow and power-inefficient due to continuous current flow through the resistors[8]. Buffer amplifiers amplify and shift signals to higher voltage levels. These are effective at maintaining signal integrity but tend to consume more power and occupy a significant area. Emerging Solutions and Innovations. The dynamic landscape of IC design demands innovations to address the

limitations of traditional voltage level shifting techniques. One emerging approach gaining traction is the use of current mirrors, a well-established concept in analog and mixed-signal IC design. Current Mirror-Based Approaches Current mirror-based voltage level shifting leverages the fundamental principles of current mirrors to enable efficient and accurate voltage translation. By replicating input currents, these approaches offer a faithful representation of input signals across varying voltage domains[14]. This innovation holds the promise of enhancing signal integrity, reducing power consumption, improving signal speed, and minimizing voltage drop. These advantages make current mirror-based solutions compelling for a wide range of applications, from low-power IoT devices to high-performance computing systems.

Voltage level shifting is a critical operation in integrated circuit design, ensuring the seamless interaction of digital and analog components. While traditional methods have served their purpose, the rapidly evolving landscape of technology and the demands of various applications necessitate innovative voltage-level shifting techniques. Current mirror-based approaches and other emerging solutions have the potential to reshape the field, offering more efficient and versatile voltage translation methods[15]. Continued research and exploration in this direction are essential to meet the evolving demands of integrated circuit design, ensuring compatibility and efficiency in an increasingly diverse and voltage-fragmented landscape.

### III. Methodology

Voltage level shifting is a crucial operation in integrated circuit design to enable seamless communication between components operating at different voltage domains. This methodology outlines the steps to implement voltage level shifting techniques using Cadence, a popular Electronic Design Automation (EDA) tool. Define the voltage level shifting requirements, including input and output voltage levels, current requirements, and frequency constraints. Identify the specific components that require voltage level shifting in your circuit. Launch Cadence's schematic capture tool (e.g., Virtuoso). Create a new project and add your schematic as shown in Figure 1. Design the schematic including the voltage level shifting components (e.g., level shifters, buffers, or current mirrors). Ensure proper connectivity and labelling of nodes with their voltage levels. Choose appropriate voltage-level shifting components from Cadence's component library or design custom components as needed[16]. Verify that the selected components meet the voltage and current requirements of your circuit.

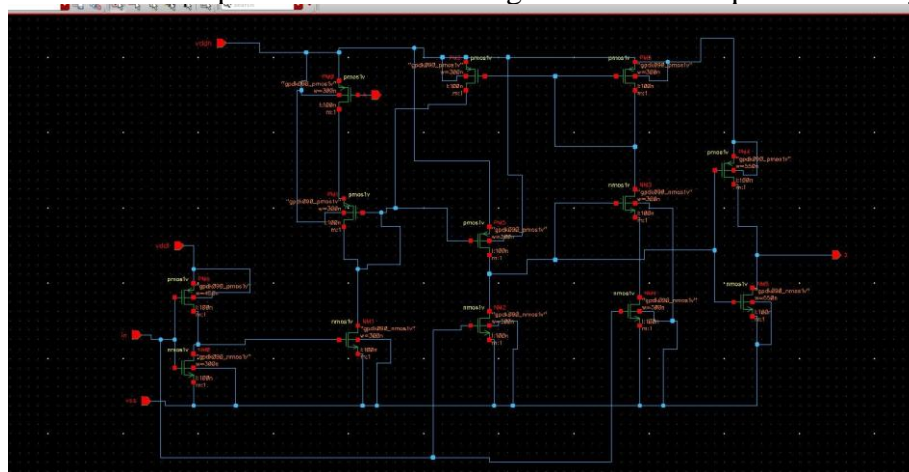


Figure 1. Schematic of the proposed level shifter

Define simulation profiles (e.g., transient, DC, or AC) to assess the performance of the voltage level shifting circuit. Specify input signals and voltage sources for simulations. Set up simulation analyses to assess signal integrity, power consumption, and voltage translation. Run simulations to verify the schematic's functionality. Analyze simulation results to ensure that the voltage level shifting meets the defined specifications. Address any issues or discrepancies identified during the simulation. Create the physical layout of the circuit using Cadence's layout tool (e.g., Virtuoso Layout XL). Follow design rules and guidelines to ensure proper component placement and routing. Perform post-layout simulations to account for parasitic effects, signal integrity, and any layout-related issues. Make necessary adjustments to the layout based on simulation results. Conduct thorough design verification to ensure that the voltage level shifting circuit meets the required specifications [17-18]. Verify that the voltage translation is accurate, and the circuit operates within acceptable margins. Optimize the design for factors such as power efficiency, speed, and area utilization. Iterate through the design and simulation steps if necessary to achieve the desired performance[19]. Prepare comprehensive documentation including schematics, layouts, simulation results, and design files for future reference and collaboration [20]. If required, move forward with the fabrication and testing of the physical IC. Validate the IC's performance by comparing measured results with simulation expectations. This methodology provides a structured approach to implementing voltage level shifting techniques in integrated circuit design using Cadence. Adapt and refine the steps according to your specific project requirements and Cadence toolset. Additionally, always adhere to best practices and guidelines provided by Cadence for the most accurate and reliable results.

#### IV. Results and Conclusion

The simulation of level shifter circuit done for measuring different parametric results. Expected Results in Cadence for Voltage Level Shifting Techniques are Signal Integrity Analysis, Verify that the voltage level shifting circuit accurately translates input signals from one voltage domain to another. Confirm that the output signals meet the voltage specifications and maintain their integrity throughout the transition. Power Consumption Analysis, Measure the power consumption of the voltage level shifting circuit. Evaluate power efficiency and ensure that it operates within acceptable power limits, especially in low-power applications like IoT devices.

Speed and Delay Analysis, Assess the speed of the voltage translation process. Calculate signal propagation delay through the level shifting circuit. Ensure that the circuit meets timing requirements, especially in high-speed applications. Voltage Drop Analysis, Analyze voltage drop across the voltage level shifting components. Ensure that voltage levels at the output accurately reflect the input specifications without significant voltage loss. Noise and Distortion Analysis, Evaluate the presence of noise or distortion in the output signals. Verify that the voltage level shifting process does not introduce unwanted noise or artifacts.

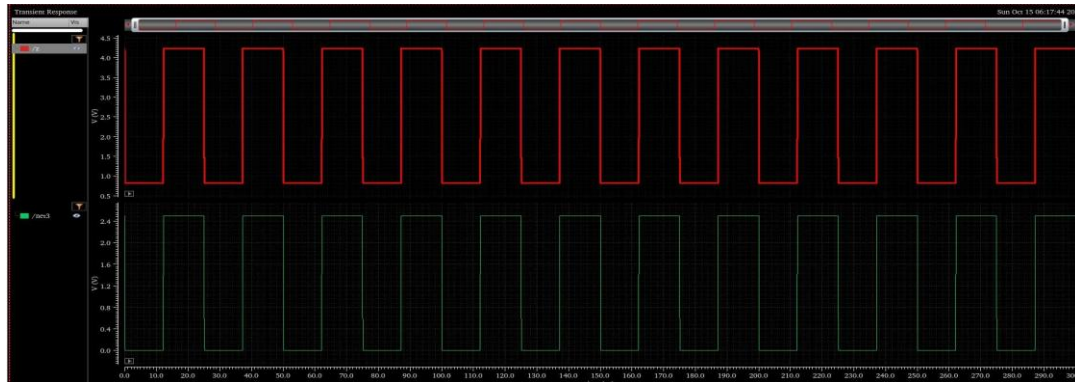


Figure 2. Transient analysis of level shifter

Parasitic Effects Analysis, Account for parasitic effects introduced by the physical layout of the circuit. Verify that the layout does not negatively impact the performance of the voltage level shifting circuit. Monte Carlo Analysis, If your design is sensitive to process variations, perform Monte Carlo simulations to assess how the voltage level shifting circuit performs under different manufacturing conditions. Sensitivity Analysis, Investigate the sensitivity of the circuit to variations in component values or environmental conditions. Trade-Off Analysis, Explore trade-offs between power consumption, speed, area utilization, and signal integrity. Determine the optimal configuration based on your project's specific requirements. Validation against Specifications, Compare simulation results against the predefined specifications and design goals to ensure that the voltage level shifting circuit meets the desired criteria. It's essential to iterate through the design, simulation, and optimization phases to achieve the desired performance and functionality for your specific application. The actual results will depend on the circuit configuration, component selection, and design constraints. The results achieved in this work are efficient compared to existing level shifter circuits.

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