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Space Vector Pulse width Amplitude Modulation for a Voltage Source Inverter for distortion free IntermittentRenewable Soures Grid Integration

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This paper introduces a novel Space Vector Pulse Width Amplitude Modulation (SVPWAM) technique tailored for a buck–boost voltage/current source inverter. Comparative analysis with conventional Sinusoidal Pulse Width Modulation (SPWM) reveals an 87% reduction in switching loss for the voltage source inverter and a 60% reduction for the current source inverter. Concurrently, the power density experiences a 2 to 3-fold increase. Furthermore, empirical validation demonstrates that the output harmonic distortions of SVPWAM are lower than those of SPWM, utilizing only one-third of the latter's switching frequency. Consequently, employing SVPWAM renders the buck–boost inverter suitable for applications necessitating high efficiency, elevated power density, tolerance to high temperatures, and cost-effectiveness. Prominent applications encompass electric vehicle motor drives or engine starter/alternator systems. Index Terms—Buck-boost, SVPWAM, reduction in switching loss, Total Harmonic Distortion (THD)

.I.INTRODUCTION

CURRENTLY, two existing inverter topologies are used for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional three-phase inverter with a high voltage battery and a three-phase pulsewidth modulation (PWM) inverter with a dc/dc boost front end. The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor's constant power speed range (CPSR), which can be alleviated through the dc–dc boosted PWM inverter.

Fig. 1 shows a typical configuration of the series plug-in electric vehicle (PHEV). The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed [1]–[3]. Active switching rectifier or a diode rectifier with small

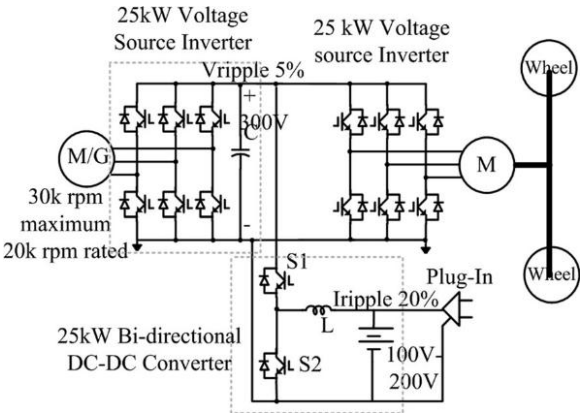

Fig. 1. Typical configuration of a series PHEV.

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DC link capacitor has been proposed in [4], [5], [8]–[12]. Varies types of modulation method have been proposed previously such as optimized pulse-width-modulation [13], improved Space-Vector-PWM control for different optimization targets and applications [14]–[16], and discontinuous PWM (DPWM) [17]. Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples [18]. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if an equal output THD is required, DPWM cannot reduce switching loss than SPWM. Moreover, it will worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been proposed in [6] and [7] to reduce the period of PWM switching to only 1/3 of the whole fundamental period. However, these papers didnt compare the spectrum of this method with others, which is not fair. In addition, the method is only specified to a fixed topology, which can not be applied widely.

This paper proposes a novel generalized space vector pulsewidth amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI) and current source inverter (CSI). By eliminating the conventional zero vector in the space vector modulation, two-third and one-third switching frequency reduction can be achieved in VSI and CSI, respectively. If a unity power factor is assumed, an 87% switching loss reduction can be implemented in VSI, and a 74% reduction can be implemented in CSI. A 1-kW boost-converter inverter system has been developed and tested based on the SVPWAM method. A 90% power loss reduction compared to SPWM has been observed. The two stage efficiency reaches 96.7% at the full power rating. The power volume density of the prototype is 2.3 kW/L. The total weight of the system is 1.51 lb. Therefore, a

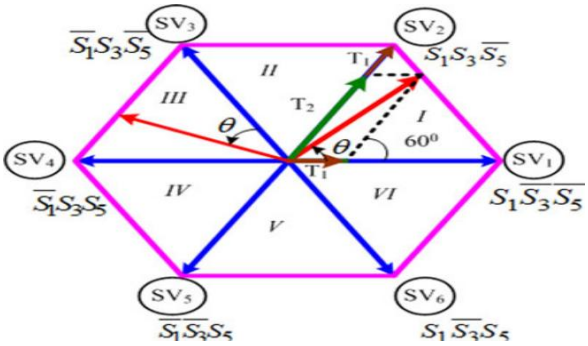

Fig. 2. SVPWAM for VSI.

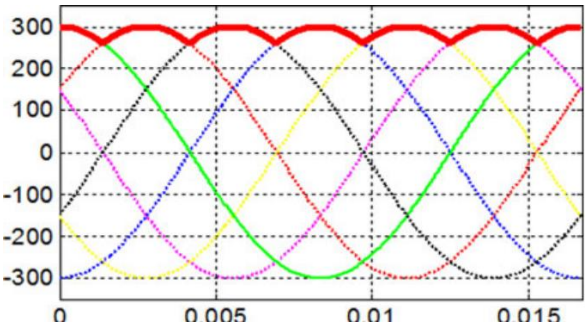

Fig. 3. DC-link voltage of SVPWAM in VSI.

high-efficiency, high-power density, high-temperature, and lowcost 1-kW inverter is achieved by using an SVPWAM method.

II. SVPWAM FOR VSI

A.Principle of SVPWAM Control in VSI

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The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig. 2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore, S1 and S2 keep constant ON, and S3 and S6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage Vac at this time. Consequently, the dc-link voltage should present a 6ω varied feature to maintain a desired output voltage. The corresponding waveform is shown in solid line in Fig. 3. A dc–dc conversion is needed in the front stage to generate this 6ω voltage. The topologies to implement this method will be discussed later. The original equations for time period T1 and T2 are

$$T_1 = \frac{\sqrt{3}}{2} m \sin\left(\frac{\pi}{3} - \theta\right); \quad T_2 = \frac{\sqrt{3}}{2} m \sin(\theta) \tag{1}$$

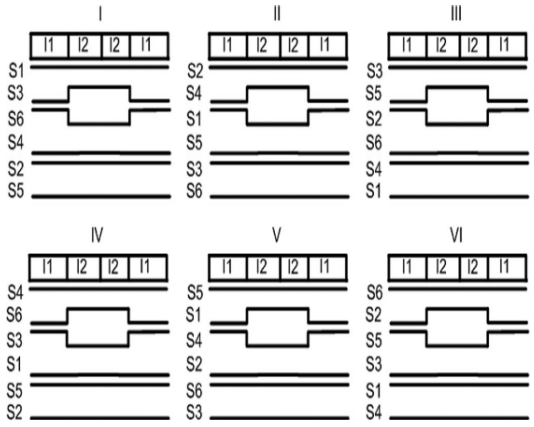

Fig. 4. Vector placement in each sector for VSI.

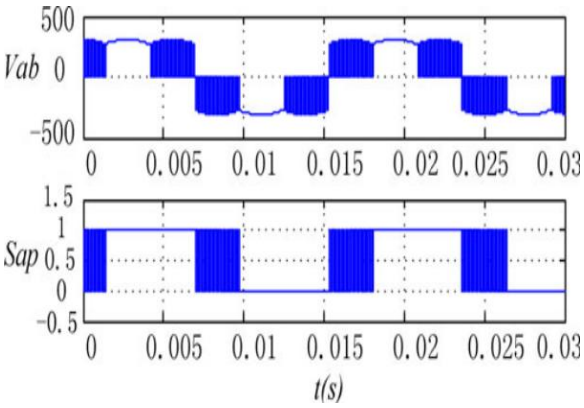

Fig. 5. Theoretic waveforms of dc-link voltage, output line-to-line voltage and switching signals.

where θ ∈ [0,π/3] is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and mutifrequency output harmonics. Therefore, in order to keep the switching period constant but still keep the same pulsewidth as the original one, the new time periods can be calculated as

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$$T_1'/T_s = T_1/(T_1 + T_2) \quad (2)$$

The vector placement within one switching cycle in each sector is shown in Fig. 4. Fig. 5 shows the output line-to-line voltage and the switching signals of S1 .

B. Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within [−60◦, 60◦], at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage VDC , and the current stress is equal to output current ia . Thus the switching loss for each switch is

$$\begin{aligned} P_{\mathrm{SW\_I}} &= \frac{1}{2\pi}\left[\int_{-\pi/6}^{\pi/6} E_{\mathrm{SR}} \frac{|I_m \sin(\omega t)| \cdot V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} \cdot f_{\mathrm{sw}}\, d\omega t \right. \\ &\quad \left. + \int_{5\pi/6}^{7\pi/6} E_{\mathrm{SR}} \frac{|I_m \sin(\omega t)| \cdot V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} \cdot f_{\mathrm{sw}}\, d\omega t \right] \\ &= \frac{2-\sqrt{3}}{\pi} \cdot \frac{I_m V_{\mathrm{DC}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} E_{\mathrm{SR}} \cdot f_{\mathrm{sw}}, \end{aligned} \quad (3)$$

where *E*SR, *V*ref , *I*ref are the references.

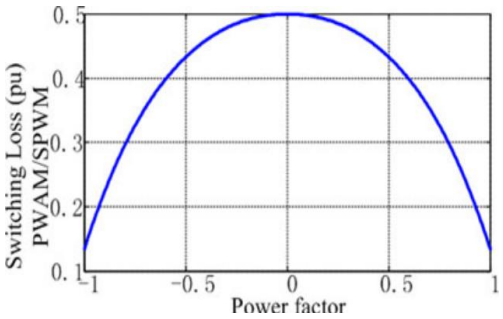

Fig. 6. (SVPWAMpower loss/SPWM power loss) versus power factor in VSI.

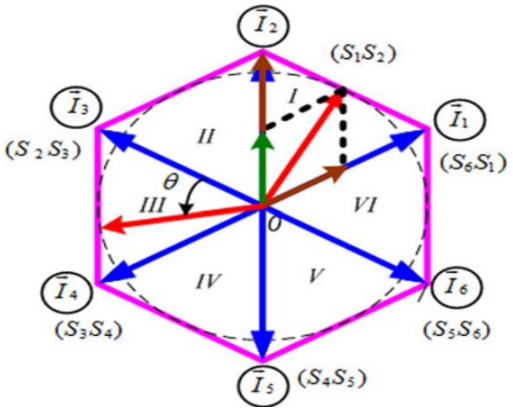

Fig. 7. Conventional CSI and its corresponding SVPWAM diagram.

Since the SVPWAM only has PWM switching in two 60◦ sections, the integration over 2π can be narrowed down into integration within two 60◦

$$P_{\mathrm{SW\_I}} = (2\sqrt{3})/\pi \cdot (I_m V_{\mathrm{DC}}/(V_{\mathrm{ref}} I_{\mathrm{ref}})) \cdot E_{\mathrm{SR}} \cdot f_{\mathrm{sw}}. \quad (4)$$

The switching loss for a conventional SPWM method is

$$P_{\mathrm{SW\_I'}} = (2/\pi) \cdot (I_m V_{\mathrm{DC}}/(V_{\mathrm{ref}} I_{\mathrm{ref}})) \cdot E_{\mathrm{SR}} \cdot f_{\mathrm{sw}}. \quad (5)$$

In result, the switching loss of SVPWAM over SPWM is f = 13.4%. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases as Fig. 6 shows. As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50–87%.

III. SVPWAM FOR CSI

A.Principle of SVPWAM in CSI

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The principle of SVPWAM in CSI is also to eliminate the zero vectors. As shown in Fig. 7, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are conducting together at any moment. Thus, for each switch, it only needs to do PWM

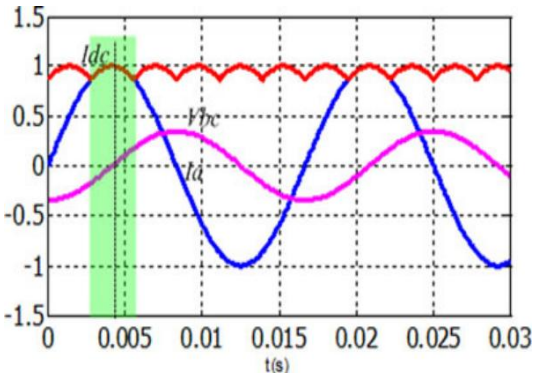

Fig. 8. Switching voltage and current when pf = 1.

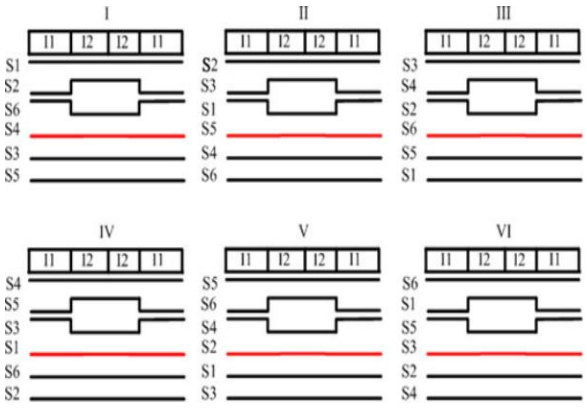

Fig. 9. Vector placement for each sector for CSI.

switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selected in each sector, this method brings down the switching frequency by one-third.

Similarly, the dc-link current in this case is a 6ω varied current. It is the maximum envelope of six output currents: Ia ,Ib ,Ic , −Ia , −Ib , −Ic , as shown in Fig. 8. For example, in sector I, S1 always keeps ON, so the dc-link current is equal to Ia . The difference between dc-link current in CSI and dc-link voltage in VSI is dc-link current in CSI is overlapped with the phase current, but dc-link voltage in VSI is overlapped with the line voltage, not the phase voltage.

The time intervals for two adjacent vectors can be calculated in the same way as (1) and (2). According to diagram in Fig. 7, the vector placement in each switching cycle for six switches can be plotted in Fig. 9.

The SVPWAM is implemented on conventional CSI through simulation. Fig. 10 shows the ideal waveforms of the dc current Idc , the output phase ac current and the switching signals of S1 . The switching signal has two sections of PWM in positive cycle, but no PWM in negative cycle at all.

B. Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dclink current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig. 8 Thus, the switching loss for a single switch is determined by

$$P_{SW\_CSI} = \frac{2-\sqrt{3}}{\pi}\frac{\overline{i_{dc}}\cdot V_{l-lpeak}}{V_{ref}I_{ref}}E_{SR}f_{sw}. \quad (6)$$

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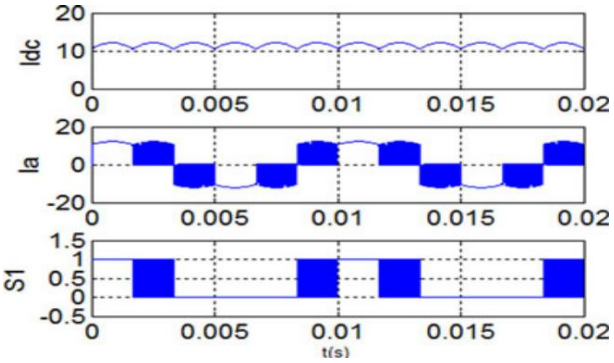

Fig. 10. Theoretic waveforms of dc-link current, output line current and switching signals

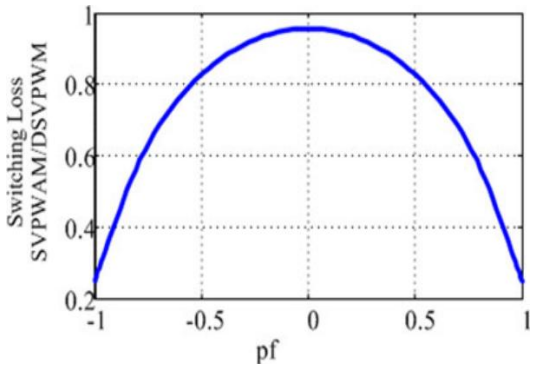

Fig. 11. CSI switching loss ratio between SVPWAM and discontinuouse SVPWM versus power factor.

When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result in (6). The corresponding switching loss ratio between SVPWAM and discontinuous SVPWM is shown in Fig. 11.

IV. SPECTRUM ANALYSIS OF SVPWAM

A fair comparison in switching loss should be based on an equal output harmonics level. Thus, the switching loss may not be reduced if the switching frequency needs to be increased in order to compensate the harmonics. For example, discontinuous SVPWM has to have double switching frequency to achieve the same THD as continuous PWM. So the switching loss reduction is much smaller than 50%. Therefore, for the newly proposed SVPWAM, a spectrum analysis is conducted to be compared with other methods on the basis of an equal average switching frequency, which has not been considered in paper [16].

A.SPECTRUM COMPARISON BETWEEN SVPWAM, SPWM, AND SVPWM

The object of spectrum analysis is the output voltage or current before the filter. The reason is that certain orders of harmonics can be eliminated by sum of switching functions in VSI or subtraction of switching functions in CSI. The comparison is between SVPWAM, DPWM, and continuous SVPWM in VSI/CSI. The switching frequency selected for each method is different, because the comparison is built on an equalized

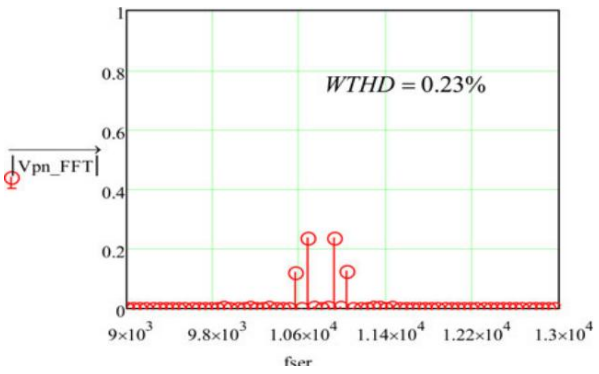

Fig. 12. Spectrum of SPWM at switching frequency.

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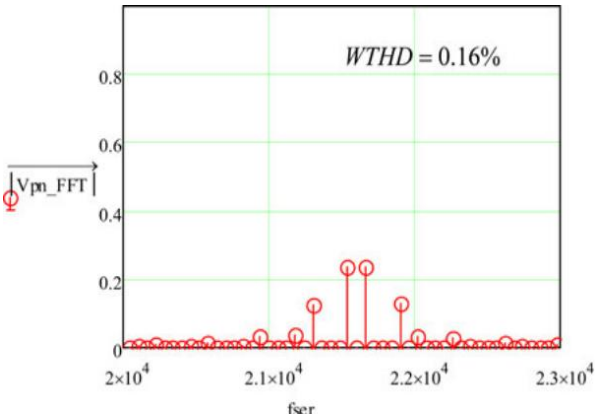

Fig. 13. Spectrum of discontinuous SVPWM at switching frequency.

average switching frequency over a whole fundamental cycle, in order to make the harmonics comparable at both low modulation and high modulation range. Assume that the base frequency is f0 = 10.8 kHz. Thus, 3f0 should be selected for SVPWAM, and f0 should be selected for continuous SVPWM in VSI. In CSI, 3f0 , 2f0 , and f0 should be selected for SVPWAM, discontinuous SVPWM, and continuous SVPWM, respectively.

The modulation index selected here is the maximum modulation index 1.15, since the SVPWAM always only has the maximum modulation index. Theoretically, the THD varies with modulation index. The dc-link voltage is designed to be a constant for SVPWM and an ideal 6ω envelope of the output six line-to-line voltages for SVPWAM. Thus, the harmonic of the SVPWAM here does not contain the harmonics from the dc–dc converter output. It is direct comparison between two modulation methods from mathematics point of view.

Figs. 12–14 show the calculated spectrum magnitude at first side band of switching frequency range for three methods. It can be concluded that the ideal switching function of SVPWAM has less or comparable harmonics with SPWM and DPWM.

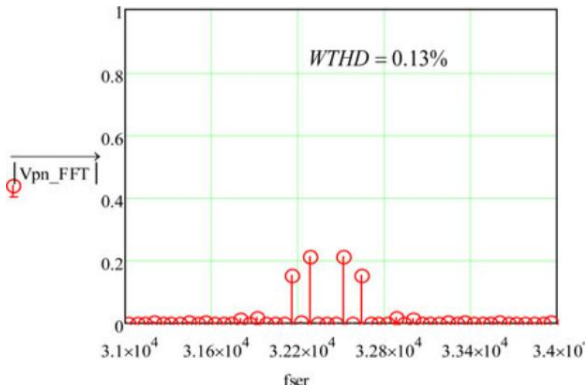

Fig. 14. Spectrum of SVPWAM at switching frequency.

V. TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a 6ω varied dc-link voltage or current; VSI or CSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter.

The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current Ipn to have a constant average value, the open zero state duty cycle Dop will be regulated instantaneously to control Ipm to have a 6ω fluctuate average value, resulting in a pulse

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type 6ω waveform at the real dc-link current Ipn , since I1 is related to the input dc current Iin by a transfer function

$$I_1 = \frac{1 - D_{op}}{1 - 2D_{op}} I_{in} \quad (9)$$

VI.SIMULATION RESULTS AND DISCUSSION:

A.SIMULINK BLOCK DIAGRAM :

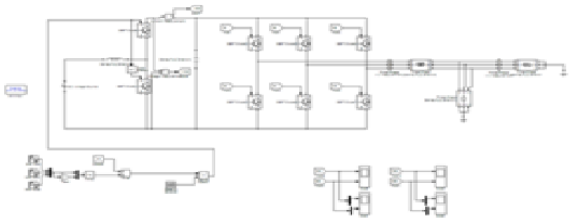

Fig15.Block Diagram of VSI

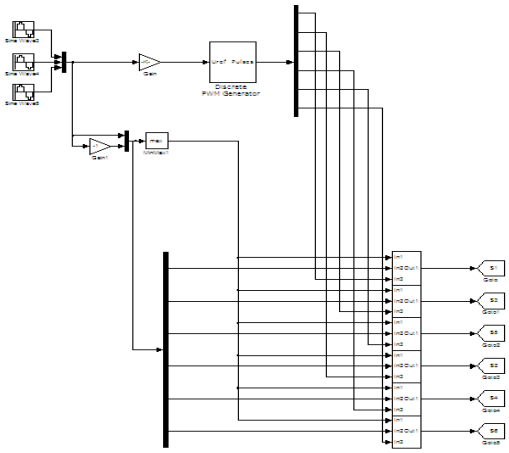

Fig 16.control diagram of svpwam

B. SIMULATION OUTPUT VOLTAGES AND CURRENTS:

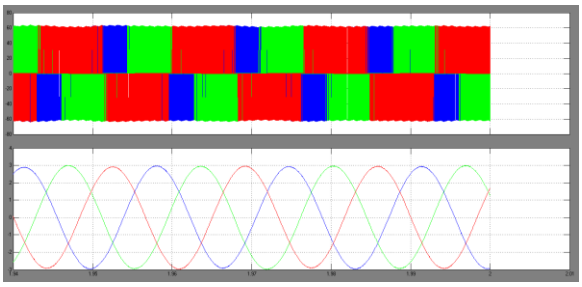

Fig 17. Output Voltage and Current using SPWM

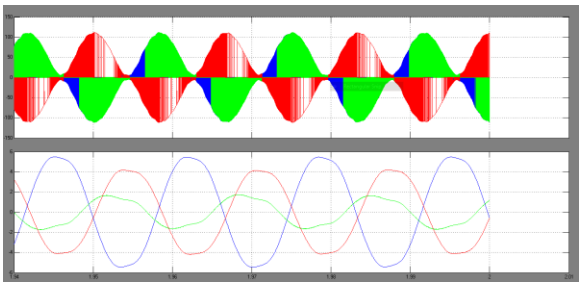

Fig 18.Output Voltage and Current using Discontinuous SVPWM

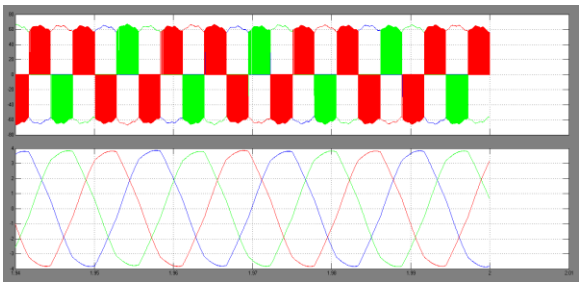

Fig 19.Output Voltage and Current using SVPWM

C.FFT ANALYSIS OF VOLTAGES:

1.Using Sinsoidal PWM:

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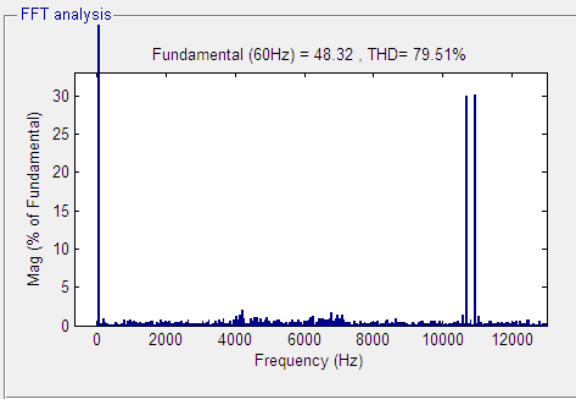
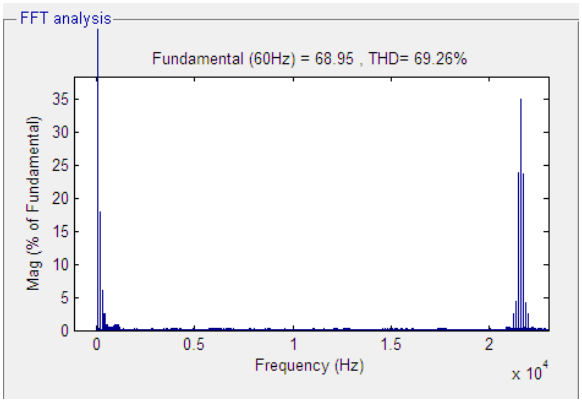
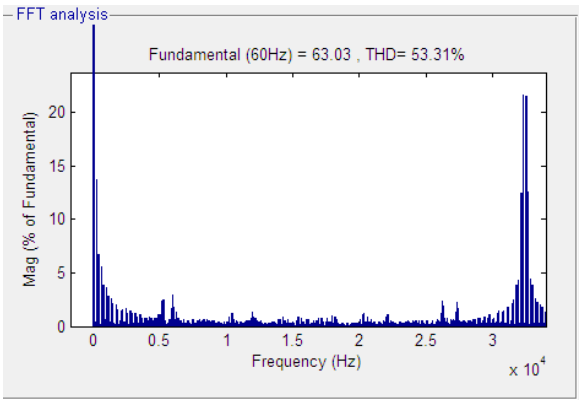


2.Using Discontinuous SVPWM:



3.Using Space Vector PWM



By observing the above FFT analysis,it is clear that the Total Harmonic Distortion is mitigated from 79.91% to 53.31% by using Space Vector Pulse width Modulation Technique**.**

VII. CONCLUSION

The SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.

2) The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6 μF) and small heat sink is needed.

3) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

A high-efficiency, high-power density, high-temperature, and low-cost 1-kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses has been validated by the simulation results that were obtained from the laboratory scale prototype.

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