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DESIGN OF FIVE-LEVEL ONE-CAPACITOR BOOST MULTILEVEL INVERTER

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ABSTRACT:
Power electronic converters play a crucial role in low power Renewable Energy Generation Systems (REGS). This study proposes a novel use for a single-phase grid-connected one-capacitor boost multilevel inverter in REGS. Multilevel inverter systems are well-suited for medium and high power applications. This research introduces a novel boost multilevel inverter that is based on a single capacitor and has five voltage levels (2Vdc, Vdc, 0, -Vdc, -2Vdc). The suggested configuration of the formation consists of a single-phase system with one direct current source, eight switches, and one capacitor. In order to enhance its power production, the inverter operates according to the principles of charge-pump theory. This involves charging the capacitor in parallel and discharging it in series connections to provide a greater voltage output. The suggested setup involves straightforward control duties. To accomplish this, a level-shift pulse width modulation approach is used. In this strategy, the reference signal is compared with four carriers to drive the switches and create the necessary pulse pattern. The created inverter has many unique characteristics, including the use of a single dc-source and one capacitor, a small dimension, simple control needs, and the capability to enhance. The MATLAB software is used to model the system and construct a simulation to assess the performance of the five-level configuration grid linked solar system.

I.INTRODUCTION

Renewable energy systems sometimes need the conversion of direct current (dc) to alternating current (ac) in order to provide ac output with certain amplitude, frequency, and minimal harmonic profile. The dominant ac/dc power electronic interfaces consist of pulse width modulation (PWM) inverters, which may be configured as two-level or multilayer systems. They allow for precise control of the amplitude, frequency, and harmonics of the output voltage. Multilevel inverter topologies provide alternating current (AC) output with decreased harmonic components. Therefore, the literature extensively discussed multilayer inverter topologies because of their advantages, such as a compact filter size and enhanced output waveform [1-9]. A multilevel inverter employs power semiconductors to generate a staircase waveform by using several DC voltage levels. Compared to typical inverters with two levels, multilayer inverters provide enhanced harmonic profile and decreased voltage strains on semiconductors [10]. The power quality of a multilayer inverter improves as the number of levels increases. Conversely, higher levels result in a significant quantity of power semiconductors and their corresponding driving circuitries. Therefore, the cost and complexity of the system are elevated. This has an impact on the dependability and effectiveness of the system [10, 11]. Several different configurations of multilayer inverters

were created. The designs mentioned include neutral point clamped (NPC), cascaded H-bridge (CHB), flying capacitor (FC), and modular multilevel converters [12–15]. The multilevel systems may be adjusted to provide output voltages at 3, 5, 7, or any desired number of levels [16]. The NPC inverter was developed by Akira Nabae and Akagi [17] as a three-level diode clamped configuration for motor driving. The stability and balancing of the dc-capacitors provide a significant challenge in this topology, despite the presence of just one dc-source. In order to maintain stability and balance in the two stacks, the voltage and current of the dc-capacitors are regulated by the dc-source. Instead of using a clamping diode, Stillwell and Pilawa-Podgurski [19] used a flying capacitor (FC) to regulate the voltage of a specific capacitor voltage-level. This capacitor voltage-level is part of an FC multilevel converter. The FC multilevel inverter has unique characteristics compared to the NPC equivalent, namely in terms of phase redundancies. This function provides the FC with the ability to charge or discharge with flexibility, and to overcome voltage imbalances or failures. Furthermore, redundancy enhances the voltage strains experienced by the power switches and improves the harmonic profile. However, the FC multilayer inverter is plagued by other limitations, including the difficulty of controlling the voltage of all capacitors and a low switching efficiency [15, 18]. The CHB multilevel converter is a kind of multilevel inverter that consists of h-bridge inverters linked in series. Every bridge is equipped with its own direct current source. The modular design of this arrangement provides a clear benefit over neutral point and FC topologies. It allows the inverter to have considerable flexibility in fault tolerance and the ability to operate at low power levels even after a cell failure [20]. The modular multilevel inverter, often known as scalable technology, is an alternative power arrangement for multilevel inverters. Submodules with autonomous control systems are interconnected in a cascade configuration to provide the desired number of levels. Nevertheless, the existing flow of electric current in the converter amplifies the total amount of energy lost by conduction in the system. The primary challenge in managing modular multilevel topologies is ensuring that the submodule capacitor remains balanced. This paper introduces a novel five-level boost inverter. The literature presents many configurations consisting of five levels. The five-level arrangement, as described in reference [21], is capable of producing a five-level output using six switches, two diodes, and two capacitors. Despite having a smaller number of switches, this system necessitates a sophisticated management algorithm to maintain balance between the capacitors and diodes, resulting in a decline in total system efficiency.

The setup described in reference [22] is similar to the one given in reference [21], since it utilizes the switched capacitors cell, but is specifically intended to produce nine levels instead of five levels. Roy et al. [23] designed a cross-switched inverter using switched-capacitor converters. This inverter employs an optimal amount of switches. However, its five-level version requires two capacitors, which increases the complexity of control. A different and unique five-level structure is introduced in reference [24]. Generating the necessary five-level output necessitates the use of seven switches, four diodes, and two capacitors. The proposed structure is a variation of the multilayer inverter configurations suggested in references [25, 26]. The topologies described in references [25, 26] have the capability to produce a nine-level output. However, this necessitates the use of two direct

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current (DC) sources with varying voltage amplitudes. In the event of a three-phase system, six DC sources are necessary. In contrast, the version described in this research is capable of producing a five-level output voltage using just one direct current (dc) source and one capacitor. Furthermore, even in a three-phase configuration, a single dc source is sufficient to provide the desired three-phase output voltage. One additional benefit of the suggested arrangement compared to the setup in [25, 26] is its capacity to increase the output voltage to a level that is more than double the input voltage. The suggested arrangement produces a five-level output voltage with an amplitude that is double the input voltage. This is achieved utilizing just one direct current (dc) source, one capacitor, and eight power switches. The output voltage levels generated include 2Vdc, Vdc, 0, -Vdc, and -2Vdc. Figure 1 illustrates the overall schematic depiction of the proposed system.
To convert the system into a three-phase version, three capacitors and 24 power switches are required. This research will focus only on the single-phase arrangement and conduct thorough investigation. The capacitor is linked in parallel with the DC source in certain conditions in order to be charged. Subsequently, it is linked in series with the DC source to provide an output voltage level of 2Vdc. This research implements level-shift PWM (LS-PWM) to control the switches of the multilayer inverter. The reference voltage is compared with four carriers in order to obtain the necessary switching states. The research is structured in the following manner: Section 2 explores the various operating modes of the constructed multilayer boost-inverter. Section 3 examines the modulation approach, Section 4 evaluates the losses using the suggested configuration, and Section 5 presents the modeling and experimental findings.

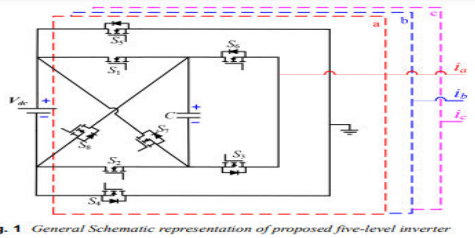

Fig. 1 *General Schematic representation of proposed five-level inverter*

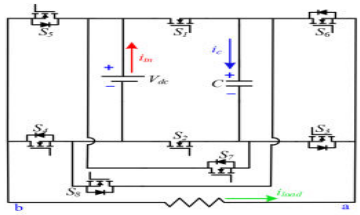

Fig. 2 *Single-phase configuration of the proposed five-level inverter*

II.PULSE WIDTH MODULATION

What is PWM?

Pulse Width Modulation (PWM) is the optimal method for achieving consistent voltage battery charging by using power device switching in the solar system controller. During PWM regulation, the current flowing from the solar array gradually decreases in response to the battery's state and recharging requirements. Examine a waveform characterized by voltage alternation between 0 volts and 12 volts. It is evident that when the voltage alternates between 12v and 0v for equal durations, a 'appropriate device' attached to

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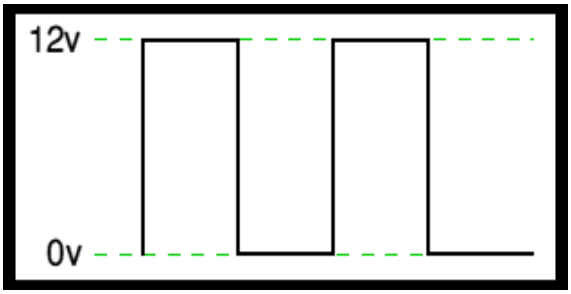
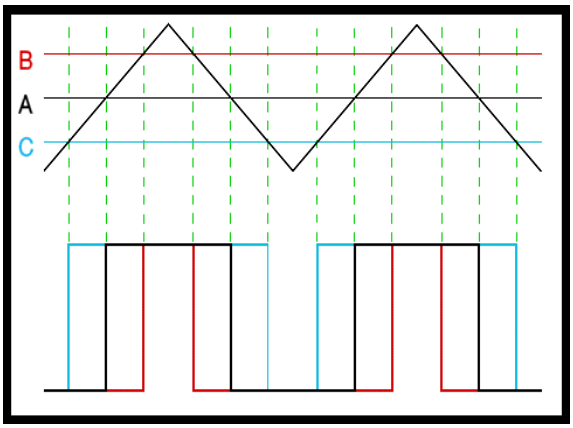
its output would perceive the average value as 6v, precisely half of 12v. By manipulating the width of the positive pulse, we may adjust the average voltage.



Pulse Width modulator

How can we produce a PWM waveform? It is rather straightforward, since there are readily accessible circuits on the TEC website. Initially, you create a triangular waveform, as seen in the figure provided. You may contrast this with a direct current voltage, which you can modify in order to regulate the desired proportion of time when the circuit is on versus off. If the voltage of the triangle is higher than the 'demand' voltage, then the output becomes high. When the triangle is positioned below the demand voltage,



III. MULTI LEVEL INVERTER

An inverter is an electrical apparatus that transforms direct current (DC) into alternating current (AC). The resulting AC may be adjusted to any desired voltage and frequency by using suitable transformers, switching mechanisms, and control circuits. Static inverters, which lack any mechanical components, find use in a diverse variety of uses. These include tiny switching power supplies in computers as well as large-scale electric utility systems that transmit high voltage direct current for the transportation of enormous amounts of electricity. Inverters are often used to provide alternating current (AC) electricity from direct current (DC) sources, such as solar panels or batteries. An electrical inverter is a robust electronic oscillator that operates at high power levels. The term "inverted" is used to describe early mechanical AC to DC converters that were designed to function in reverse, converting DC to AC.

3.1Cascaded H-Bridges inverter

Figure depicts a single phase configuration of an m-level cascaded inverter. Every individual direct current source (SDCS) is linked to a single-phase full bridge, also known as an H-bridge, inverter. The inverter level has the capability to produce three distinct voltage

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outputs: +Vdc, 0, and -Vdc. This is achieved by connecting the DC source to the AC output using various combinations of the four switches: S1, S2, S3, and S4. To generate a positive voltage (+Vdc), switches S1 and S4 are activated, whereas a negative voltage (-Vdc) may be generated by activating switches S2 and S3. When either S1 and S2 or S3 and S4 are activated, the resulting output voltage is 0. The AC outputs of each individual full bridge inverter levels are coupled in series, resulting in a synthetic voltage waveform that is the sum of the inverter outputs. The number of output phase voltage levels, denoted as m, in a cascade inverter is determined by the equation m = 2s+1, where s represents the number of distinct DC sources. The figure displays a sample phase voltage waveform for an 11-level cascaded H-bridge inverter consisting of 5 series-connected DC sources (SDCSs) and 5 complete bridges. The voltage measured over a single phase

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \quad \ldots(4.1)$$

The Fourier Transform for a stepped waveform, as shown in Figure 4.2 with s steps, may be derived as follows:

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\frac{\sin(n\omega t)}{n}, \text{ where } n = 1,3,5,7\ldots \quad \ldots(4.2)$$

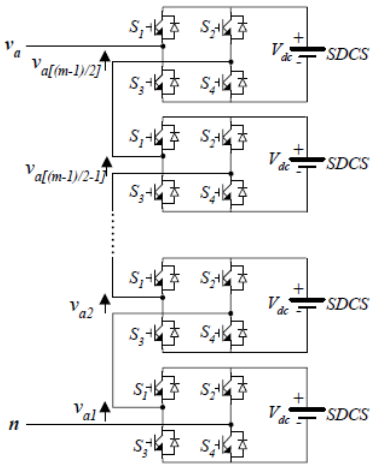

Fig.Single-phase structure of a multilevel cascaded H-bridges inverter

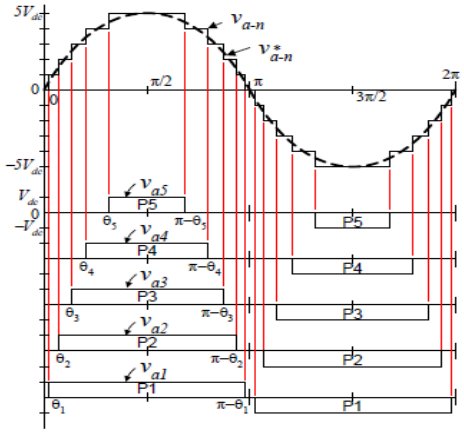

Fig. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

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IV.PROPOSED SYTEM AND CONTROL DESIGN

Proposed five-level boost multilevel inverter

Figure 2 illustrates the proposed five-level boost multilevel inverter. The suggested configuration is a five-level multilevel inverter that has the capability to enhance the output voltage to twice the input value. The implemented configuration consists of a total of eight switches, two of which lack an anti-parallel diode. Out of the 28 potential switching states of the proposed inverter, only six are actually used to produce the five-level output voltage, as shown in Table 1. Figures 3 and 4 show all the operating modes that are considered legitimate. 2.1 Operational modes In Mode 1, freewheeling takes place: the inverter produces an output voltage of zero, while capacitor C is being charged from the dc-source (see to Figure 3a). During this study, it is assumed that the capacitor is charged while the voltage across the capacitor is zero, resulting in a significant inrush current. Indeed, the majority of multilevel topologies using FCs would encounter the similar issue. For high power applications, it is possible to use a precharge device that enables the slow buildup of capacitor voltage [27–32]. Switches S1, S2, S3, and S4 are in the "on" position, while the other switches are in the "off" position. The capacitors C are being charged by the direct current (DC) source and have a voltage that is equal to the voltage of the DC source. Capacitor C is charged by the input voltage, and its steady-state value is equal to the input voltage. Output terminal an is linked to output terminal b. In Mode 2, the inverter produces an output voltage that is identical to the input voltage (refer to Figure 3b). Switches S1, S2, S3, and S5 are turned on, while the other switches are turned off. The capacitor C is charged from the direct current (dc) source and its voltage is equal to the voltage of the dc source. The positive terminal b is linked to the positive terminal of the input source, whereas terminal an is linked to the negative terminal of the dcsource. Mode 3: The inverter produces an output voltage that is double the input voltage (as shown in Figure 3c). Switches S3, S5, and S8 are turned on, while the other switches are turned off. The positive terminal b is linked to the positive terminal of the DC source, whereas terminal an is linked to the negative terminal of capacitor C. In Mode 4, freewheeling takes place. This means that the inverter produces an output voltage of zero, while capacitor C is charged from the dc-source, as shown in Figure 4a. Switches S1, S2, S3, and S4 are in the on position, while the other switches are in the off position. The capacitor C is being charged by a direct current (DC) source, and its voltage is equal to the voltage of the DC source. Capacitor C is energized by the input voltage and reaches a stable value that is equivalent to the input voltage. Output terminal b is linked to output terminal a. In Mode 5, the inverter produces an output voltage that matches the input voltage (refer to Figure 4b). Switches S1, S2, S4, and S6 are turned on, while the other switches are turned off. C is being powered by a direct current (DC) source and has the same voltage as the DC source. The positive terminal b is linked to the negative terminal of the DC source, whereas terminal an is linked to the positive terminal of the DC source. In Mode 6, the inverter produces an output voltage that is double the value of the input voltage (refer to Figure 4c). Switches S4, S6, and S7 are turned on, while the other switches are turned off. The positive terminal b is linked to the negative terminal of the direct current source, whereas terminal an is linked to the positive terminal of capacitor C. 2.2 Parameter design refers to the process of determining the values or settings of parameters in a system or model. Choosing

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the appropriate capacitance is crucial in order to minimize the amount of fluctuation in the voltage across the capacitor. A high level of fluctuation in the capacitor voltage might lead to an imbalance in the voltage steps of the output. Based on the analysis shown in Figures 3a, 3b, and 4a, it can be seen that C is connected in parallel with the direct current (dc) source and is being charged. Consequently, the subsequent equations exhibit the following characteristics:

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \qquad (1)$$

In the mode shown in Figure 4a, capacitor C is continuing to undergo the charging process. However, the present equation differs from the previously described equation and may be designated as

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \qquad (2)$$

The discharge of capacitor C occurs in the modes shown in Figures 3c and 4b. The equation governing the properties of the capacitor during these modes is

$$\{v_c = v_o - v_{dc} \Leftrightarrow i_c = i_{in} \qquad (3)$$

Figure 5 illustrates a graph representing the voltage across a capacitor. Based on the graph and information provided in (1–3), C may be chosen in the following manner:

Table 1 Switching states of the five-level inverter

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

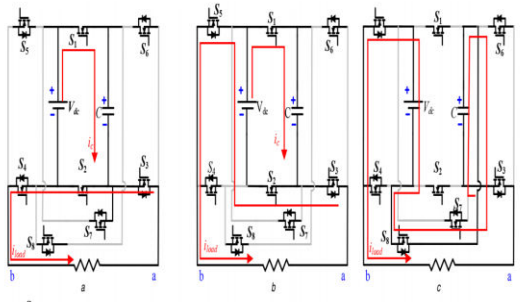

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Fig. 3 *Operation modes*
(a) Mode I, *(b)* Mode II, *(c)* Mode III

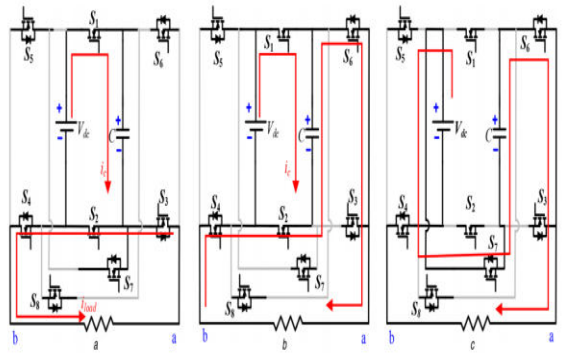
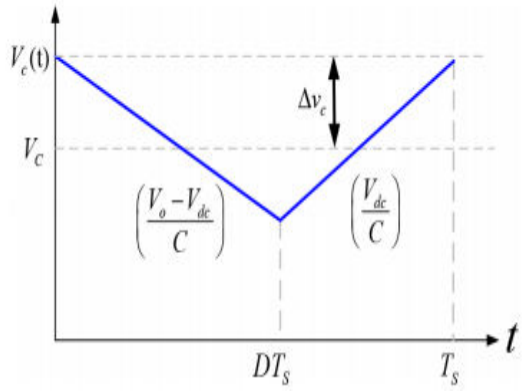


Fig. 4 *Operation modes*
(a) Mode IV, *(b)* Mode V, *(c)* Mode VI

$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c}\right) DT_s \qquad (4)$$

C is determined by the input voltage vdc, the output voltage vo, the sampling time Ts, the tolerated amount of ripple in capacitor voltage Δvc, and the duty ratio D. Table 2 provides a summary of the voltage and current pressures experienced by the components. All the switching devices experience comparable levels of current stress. Nevertheless, varying voltage stresses are seen. S7 and S8 experience the most voltage strain, which is equivalent to the output voltage. The voltage stress of the other switches is equivalent to the input voltage. It is important to acknowledge that because of the circuit's lack of symmetry, the voltage stresses on switches S7 and S8 are greater than those on the other switches. Therefore, it is crucial to give careful consideration to the selection of components.

Level shift pulse width modulation



Pulse Width Modulation (PWM) is often used to control the operation of power converters, whether they are direct current (dc) or alternating current (ac) converters, by manipulating the switches at a certain frequency of switching. The PWM block generates a pulse pattern that is designed to achieve a greater modulation index and reduce the harmonic character of the output waveform. In addition, modulation methods may be created with the purpose of minimizing switching losses, current ripple, and maintaining balanced capacitor voltage. The two-level converter utilizes a single triangular carrier waveform that is compared with the modulation signal in order to generate the switching signals pattern of the switches.

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Table 2 Devices voltage and current stress

Device	Voltage stress	Current stress
S_1	V_{in}	I_{in}
S_2	V_{in}	I_{in}
S_3	V_{in}	I_{in}
S_4	V_{in}	I_{in}
S_5	V_{in}	I_{in}
S_6	V_{in}	I_{in}
S_7	V_o	I_{in}
S_8	V_o	I_{in}

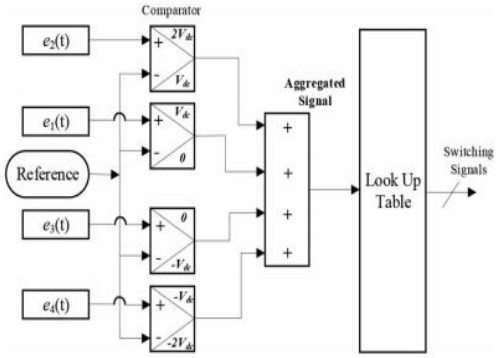

Fig. 6 *Switching signal generation schematic diagram*

V.SIMULATION RESULTS

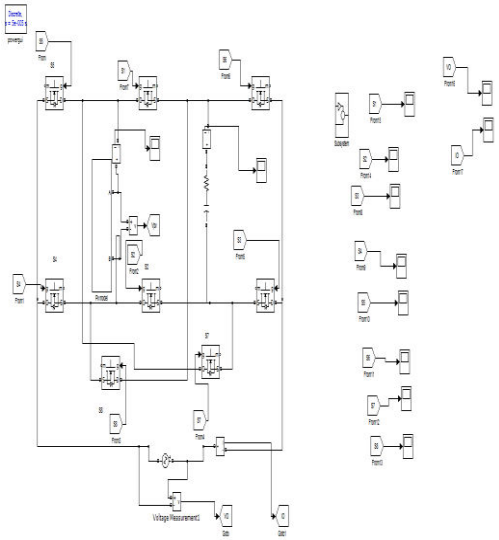

Fig .simulink model

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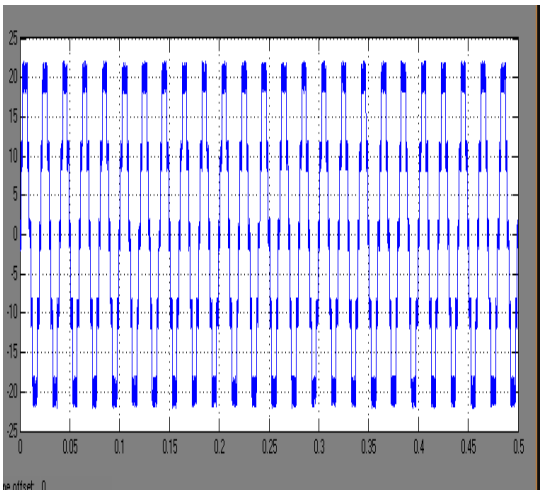
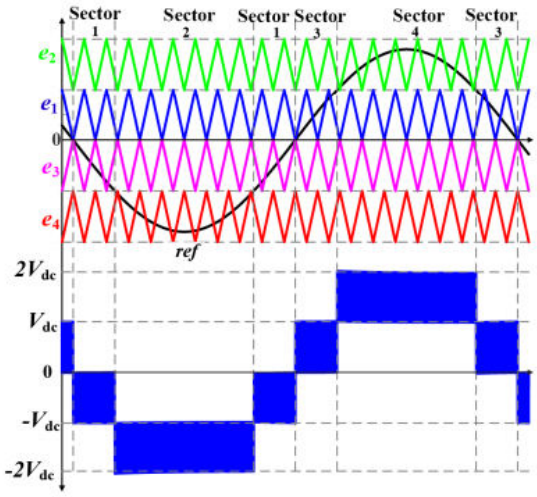


Fig grid currents

Every switching device experiences two kinds of losses: conduction losses during the device's conduction phase, and switching losses when the device transitions between the off and on states. Within each switching state, out of the eight potential states, a minimum of three switches are activated or set to the "on" position. This results in two categories of losses, namely conduction losses and switching losses. The next sections will cover the analytical computation of switching and conduction losses. 4.1 Conduction losses refer to the energy losses that occur by conduction, the process of heat transfer through a solid material or between two materials in direct contact. The suggested topology consists of eight switches, with two of them functioning as power switches that can conduct and block in only one way, while the other six switches can only block in one direction.



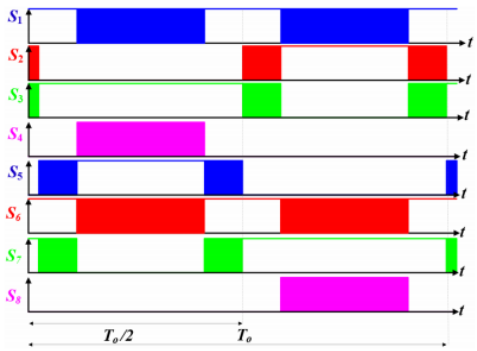


Fig. 8 *Driving signals of the five-level inverter*

The bidirectional conducting capability allows for the power switch and its body diode to conduct electricity in both directions. The instantaneous conduction losses of the power switch and its body diode may be quantified as [14, 24].

$$\rho_{c,T}(t) = [V_T + R_T i^{\alpha}(t)]i(t) \quad (5)$$

$$\rho_{c,D}(t) = [V_D + R_D i(t)]i(t) \quad (6)$$

The average conduction losses are expressed as

$$\rho_{c,avg} = \frac{1}{\Pi}\int_0^{\Pi}\left[\begin{matrix}\{N_T(t)V_T + N_D(t)V_D\}i_L(t) \\ +\{N_T(t)R_T i_L^{\alpha+1}(t)\} + \{N_D(t)i_L^2(t)\}\end{matrix}\right]d(\omega t) \quad (7)$$

The symbols ρc,T(t), ρc,D(t), VT, VD, RT, RD, α, ND, NT, and ρc, avg(t) represent the following quantities: the instantaneous conduction losses of the transistor, the instantaneous conduction losses of the diode, transistor on-state voltage drop, diode instantaneous voltage drop, transistor equivalent on-resistance, diode equivalent on-state resistance, a constant determined by transistor characteristics, number of conducting diodes, number of conducting transistors, and average conduction losses, respectively.

Switching losses

The estimation of switching losses for each switching device may be achieved by using a linear approximation of voltage and current throughout the switching period, as shown in the range of [14, 24]. The calculation of turn-on energy losses may be determined as follows:

$$E_{on,j} = \int_0^{t_{on}}\left\{\left[V_{o,j}\frac{t}{t_{on}}\right]\left[-\frac{I}{t_{on}}(t - t_{on})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{on} \quad (8)$$

Similarly, energy losses of the *j*th switch during turning off are calculated as

$$E_{off,j} = \int_0^{t_{off}}\left\{\left[V_{o,j} * \frac{t}{t_{off}}\right]\left[-\frac{I}{t_{off}}(t - t_{off})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{off} \quad (9)$$

The terms Eon, j, ton, I, Vo, and j are mentioned. Eoff, j and toff refer to the turn-on loss, turn-on time, current, voltage when turning off, turn-off loss, and turn-off time of the jth switch, respectively. The calculation of total switching power losses is possible by using the following formula:

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$$\rho_S = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{o,j} * I(t_{on} + t_{off}) f_j \right] \qquad (10)$$

Figure 9 illustrates a graph representing the efficiency of the inverter. The ideal operational power range for the suggested inverter is 350 to 650 W. Nevertheless, across the whole power range of up to 800 W, its efficiency exceeds 95%..

VI.CONCLUSION

This study presented a novel five-level boot multilevel inverter. The configuration consists of eight switches and a solitary dc-capacitor, specifically developed for a single-phase version. The gadget has the ability to generate a five-tiered output with an amplitude that is more than double the input voltage. Given that just a single capacitor is used in this configuration, the matter of balancing is not a factor of concern.
The recommended inverter's enhanced boosting capacity increases its competitiveness as a rival for PV system applications. The DC capacitor is first charged from the DC source and then reconfigured to be linked in series with the DC source. Consequently, achieving a higher output voltage is feasible. The LS-PWM approach is used for the purpose of regulating the switches of the inverter. Switching states are designed with the particular purpose of ensuring that the capacitor is charged for a sufficient amount of time, hence avoiding any major variations in the voltage of the capacitor.

Table 3 Component requirements for single-phase five-level multilevel inverter

Topology	NPC [34]	FC [19]	CHB [35]	[10]	[36]	Diode clamped [37]	Capacitor clamped [38]	This work
number of main switcheS	8	8	8	4	5	8	12	8
number of diodes	0	0	0	4	4	6	0	2
number capacitors	3	3	0	2	2	4	4	1
number of dc-source	1	1	2	1	1	1	1	1

In order to authenticate and confirm the functionality of the new system, it is replicated via the use of the MATLAB/SIMULINK platform and a tangible model is constructed inside the laboratory. The simulation results are consistent and support the analytical analysis.

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