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Design and analysis of Gate all around Tunnel FET In 10nm Technology

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Abstract. By using TCAD simulation method, we have developed GaAs/InN heterostructure-based nanowire gate-all-around (GAA) negative capacitance (NC) tunnel field-effect transistor (TFET). The proposed GAA-TFET eliminates the thermionic restriction (60 mV/decade) on the subthreshold swing (SS) of traditional MOSFETs by improved electrostatic control and quantum mechanical tunnelling. In addition, by taking use of gate voltage differential amplification when specific circumstances, An NC state ferroelectric materials enhances TFET performance. The very high ION /IOFF The most surprising results of this gadget include a ratio of 1011 and a huge on-state current of 135 A, which beats all prior results. When the NC effect is incorporated into a low ss and high voltage. The output characteristics also showed considerable drain induced by barrier lowering (DIBL) of 9.7 mV, huge transconductance (gm) of 7.87 mS (103 orders greater than the baseline TFET), and 0.53 V as the threshold voltage (37.65% less than the baseline TFET). Thus, all the findings suggest that the suggested device shape might open up new opportunities for electrical.

Keywords: Tunnel FET, MOSFET, DIBL, CMOS.

1. Introduction

Scaling complementarity of metal-oxide-semiconductor (CMOS) is in particular focusing to minimize the tool in step with-feature costs, growth pace,lower length, decrease strength consumption. cutting down the tool size in MOSFETs result have arisen a few numerous challenges including quick channel consequences (SCEs), hot provider consequences (HCEs), raising t he leakage current, drain precipitated barrier decreasing (DIBL), and reliability problems. moreover, within the case of MOSFETs, Boltzmann's tyranny imposed the restrict of inverse subthreshold slope (SS) on 60 mV/decade hindered supply voltage scaling, a technique for decreasing of power dissipation in integrated circuit applications.

Because this allows for switching of sub-kBT/q and sporadic voltage function, In the tunnel discipline-effect transistor is frequently regarded as the most promising electrical transfer for low standby power (LSTP) operation and ultra-low power devices. In recent times, Appenzeller and others acquired a tunnelling FET with a subthreshold slope from band to band is around 40 mV/dec. To update the MOSFET through TFET a few same consequences are posted via resolving the issues associated with low on contemporary. OFF at a very low level present day can also be carried out from TFET devices with the help of Si-based technology and the possibility of achieving a lower subthreshold swing.

Making a switch pace quicker and integration density growing according CMOS dimensions have consistently shrunk according to Moore's law. during the last numerous many years. because of high leakage present day for instance, off-state leaks contemporary through quick channel outcomes (SCEs), contemporary gate leakage, and junction leakage modern-day, and junction leakage contemporary, energy consumption has been rapidly elevated at the same time as CMOS era node will become smaller. For low working energy gadgets it isn't smooth to deal with supply voltage (VDD) scaling. TFET will update the all that issues that come from MOSFET.

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2. DEVICE STRUCURE:

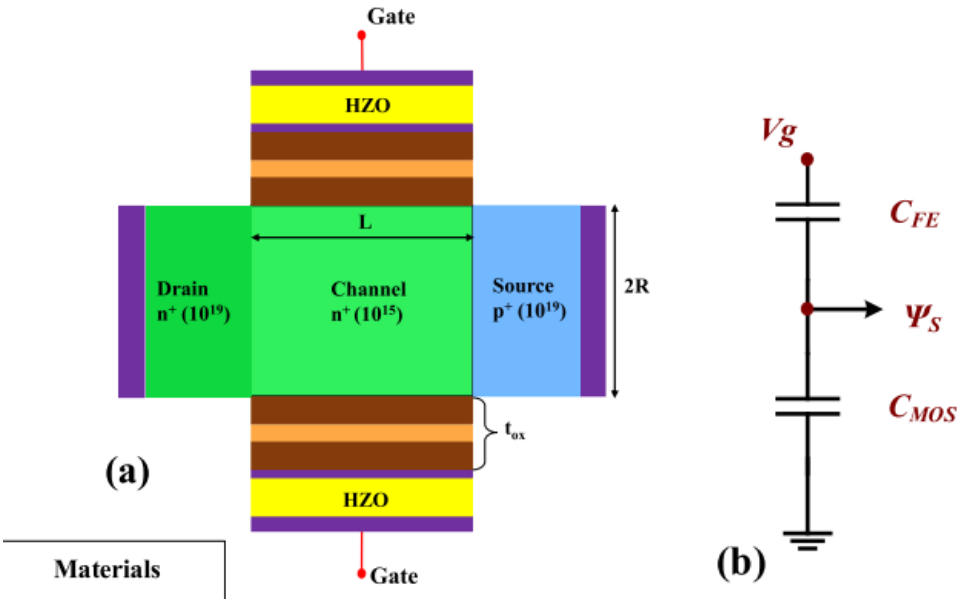
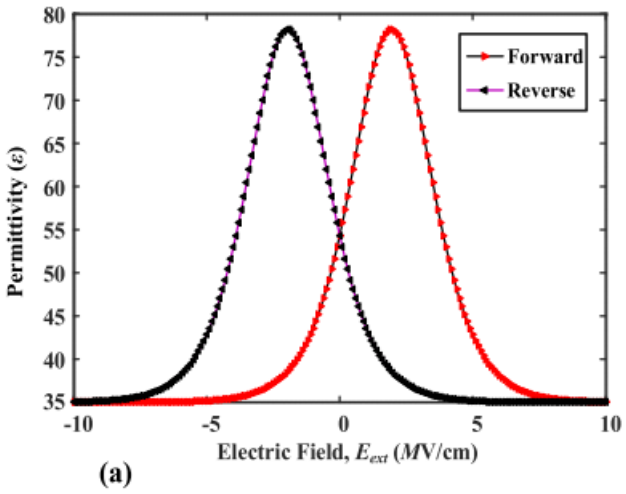


FIG-2: equivalent capacitance system, in where CFE is the sum of the capacitances of the FE layers connected in series, and CMOS

The semiconductor industry has spent decades concentrating on scaling complementary of metal-oxide semiconductor (CMOS) technology to reduce device size, speed, reduce power consumption, and lower cost-per-function. MOSFETs' device size is being reduced has led to a number of difficulties, such as higher leakage current, and reliability issues. Additionally, the Boltzmann's tyranny-imposed restriction of 60 mV/decade on the inverse subthreshold slope (SS) applies to MOSFETs. Because it enables sub-kBT /q switching and low-voltage operation, the tunnel field-effect transistor is frequently regarded as the most promising electrical switch for ultra-low power electronics and low standby power (LSTP) operation.A few days ago, Appenzeller et al. achieved a slope of subthreshold from a band to band tunnelling FET device of about 40 mV/dec [6]. Similar results are reported to use TFET in stead of MOSFET addressing the low phase current concerns.



(a) Permittivity vs. electric field curve

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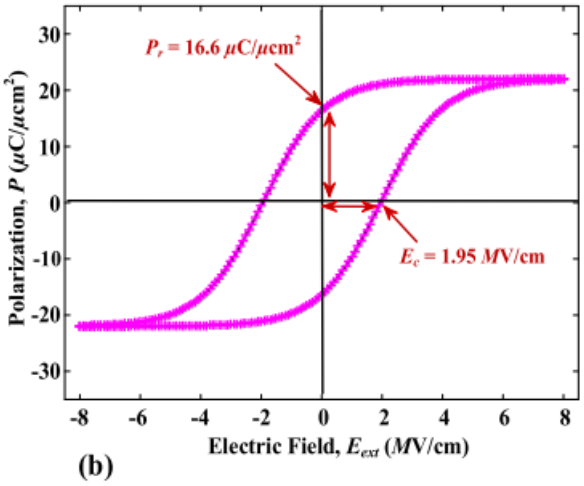
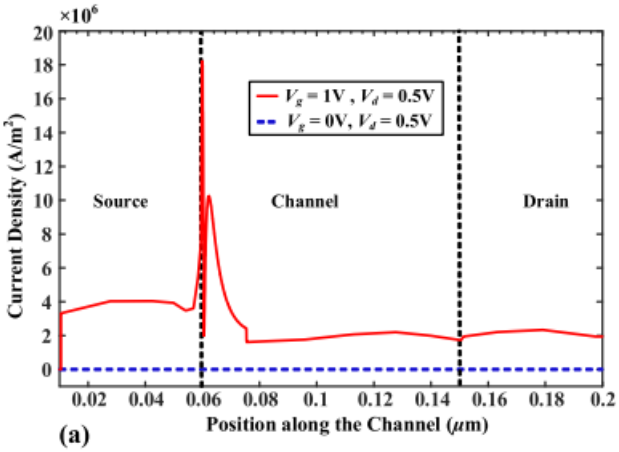


(b) polarization vs. the electric field (under the dynamic sweep) for 9nm $Hf_{0.5}Zr_{0.5}O_2FE$,

3. Results and Discussion

In this primary a part of the investigations, with the aid of using the use of a heterostructure of GaAs/InN we designed a nanowire Gate-All-round TunnelFET and not utilising a poor capacitance impact, which changed into then modified



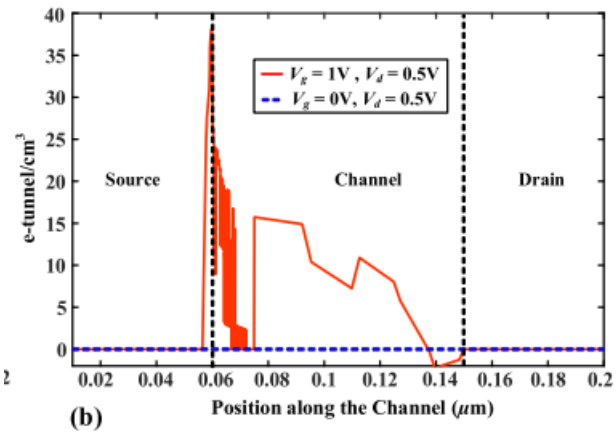


FIGURE 5. The distribution profile of the current density and e-tunneling along with the position of channel length in different gate voltages for the nanowire GAA n-channel Tunnel-FET; (a) current density vs position along the channel, showing a maximum value of 1.8×10^7 A/m² (b) e-Tunneling in logarithmic scale vs position along the channel showing the highest value of $\approx 10^{30}$/cm³.

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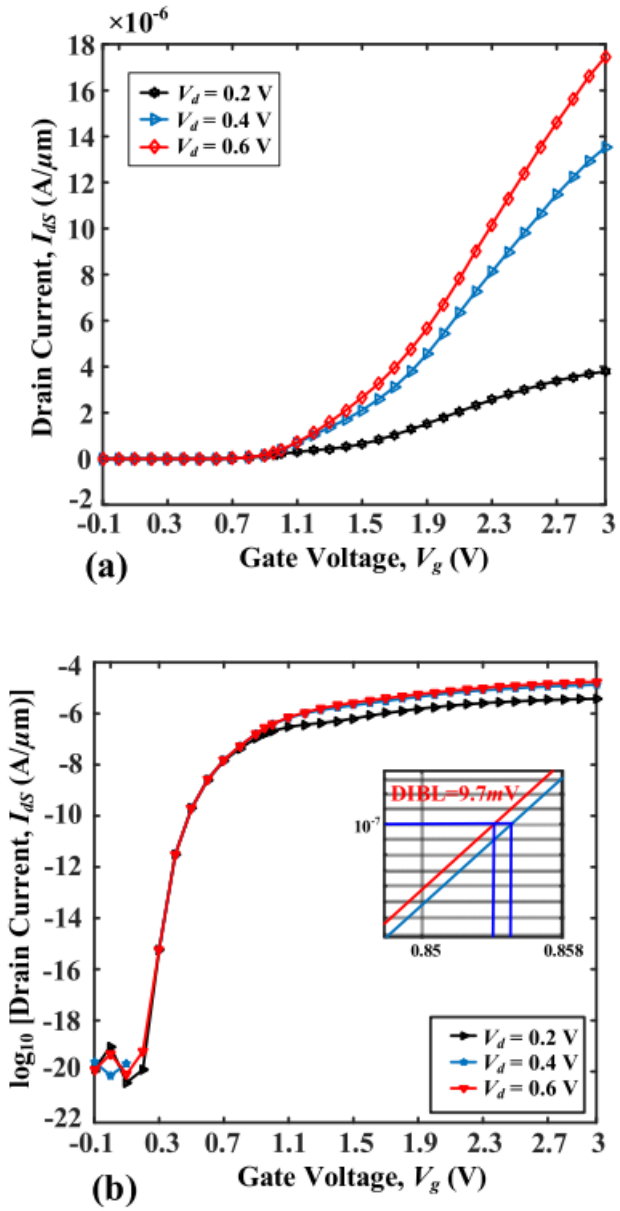

FIGURE 6. Transfer characteristics of the baseline NGAA Tunnel-FET (a) I_{ds} vs V_g, showing a large saturation current of 17 μA and a maximum I_{ON}/I_{OFF} ratio of ≈1.132 × 10^9 at V_d = 0.6V, and (b) log10 (I_{ds}) vs V_g curve by differing V_d, showing a low DIBL of 9.7 mV.

4. Conclusions

Through this study, we can understand the structure and baseline of Tunnel FET and advantages of using TFET in the case of MOSFETs. This indicates better control of channel and current capacity of CMOS devices . TFET involves training the RFR model using a variety of device characteristics from each potential fluctuated device. To forecast the ID variation, five key device parameters—namely. s. Additionally, it functions effectively by assessing the device's properties under different bias settings. The investigated ML model has therefore proven to be physics-free and highly compatible with different device circumstances. A novel voltage detector made up of a TFET and a resistor is suggested in this study. In comparison to traditional diode-based voltage detectors. GaAs/InN nanowire TFET therefore offers a special path for the continued development of the usability of electronic devices and appears to be a workable choice for a technological platform.

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With the InAs/Si TFET as an example, a novel design for TFETs is suggested, and the device properties are thoroughly examined. The following are some of the suggested architecture's benefits: First, because the gate field is parallel to the tunnelling direction, the gate control is increased, as is the electrical performance. Second, the flexibility of TFET-based circuit design is increased by the ability of our proposed devices to alter the effective tunnelling area and current in accordance with the real needs of circuit design. Third, both n-type and p-type devices may use the device design due to its improved material compatibility. Fourth, this suggested topology exhibits strong compatibility with CMOS technology without the need for challenging manufacturing procedures.

In this study, we suggested employing DMG to take advantage of within-channel tunnelling and revealed innovative features of the suggested device. Although we have shown how to use within-channel tunnelling in a silicon-based TFET, the idea may be applied to TFETs made of other materials with the right device optimization. Additionally, we have shown that within-channel tunnelling can be used for channels longer than 40 nm.

References

1. R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, 1974 ‘‘Design of ion-implanted MOSFET’s with very small physical dimensions,’’ IEEE J. Solid-State Circuits, vol. SSC-9, no. 5, pp. 256–268.
2. G. A. Brown, P. M. Zeitzoff, G. Bersuker, and H. R. Huff, 2004 ‘‘Scaling CMOS: Materials & devices,’’ Mater. Today, vol. 1, no. 7, pp. 20–25, doi: 10.1016/S1369-7021(04)00051-3.
3. G. E. Moore, Cramming More Components Onto Integrated Circuits. New York, NY, USA: McGraw-Hill, 1965.
4. L. Knoll, Q. T. Zhao, A. Nichau, S. Richter, G. V. Luong, S. Trellenkamp, A. Schäfer, L. Selmi, K. K. Bourdelle, and S. Mantl, Dec. 2013 ‘‘Demonstration of improved transient response of inverters with steep slope strained Si NW TFETs by reduction of TAT with pulsed IV and NW scaling,’’ in IEDM Tech. Dig., p. 4.
5. K. Jeon, W.-Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J.-K. Liu, and C. Hu, 2010 ‘‘Si tunnel transistors with a novel silicided source and 46 mV/dec swing,’’ in Proc. Symp. VLSI Technol., pp. 121–122.
6. G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, and P. Oakey, 2011, ‘‘Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing,’’ in IEDM Tech. Dig., pp. 33.6.1–33.6.4.
7. S. Cho, J. S. Lee, K. R. Kim, B.-G. Park, J. S. Harris, Jr., and I. M. Kang, 2011,‘‘Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors,’’ IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4164–4171.
8. M. S. Islam, S. Sadman, A. S. M. J. Islam, and J. Park, 2020 ‘‘HfO2/TiO2/HfO2 tri-layer high-K gate oxide based MoS2 negative capacitance FET with steep subthreshold swing,’’ AIP Adv., vol. 10, no. 3, Art. no. 035202.
9. W. Zhang, J.-Z. Kong, Z.-Y. Cao, A.-D. Li, L.-G. Wang, L. Zhu, X. Li, Y.-Q. Cao, and D. Wu, 2017, ‘‘Bipolar resistive switching characteristics of HfO2/TiO2/HfO2 trilayer-structure RRAM devices on pt and TiN-coated substrates fabricated by atomic layer deposition,’’ Nanosc. Res. Lett., vol. 12, no. 1, pp. 1–11.
10. E.-H. Toh, G. H. Wang, L. Chan, D. Sylvester, C.-H. Heng, G. S. Samudra, and Y.-C. Yeo, 2008 ‘‘Device design and scalability of a double-gate tunneling field-effect transistor with silicon-germanium source,’’ Jpn. J. Appl. Phys., vol. 47, no. 4S, p. 2593.

ISSN PRINT 2319 1775 Online 2320 7876

Research paper **Volume 11, Sp.Iss 6 , 2022**

11. Dimitris E. Anagnotou, Michael T. Chryssomallis, "Reconfigurable UWB antenna with RF-MEMs for on-demand WLAN Rejection", IEEE Transactions on Antennas and Propagation, Vol. 62, No. 2, Feb. 2014.
12. S. A. Aghdam, "Reconfigurable Antenna With a Diversity Filtering Band Feature Utilizing Active Devices for Communication Systems," in IEEE Transactions on Antennas and Propagation, vol. 61, no. 10, pp. 5223-5228, Oct. 2013.
13. N. Tasouji, J. Nourinia, C. Ghobadi and F. Tofigh, "A Novel Printed UWB Slot Antenna With Reconfigurable Band-Notch Characteristics," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 922-925, 2013.