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Design and Implementation of High-Speed Vedic Multiplier Architectures Using Optimized Adder Topologies for Efficient VLSI Systems

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Abstract

The evolution of VLSI design has heightened the need for high-speed, low-power, and area-efficient arithmetic units. Among these, multipliers are fundamental components in digital signal processing (DSP), microprocessors, and various computation-intensive applications. This paper presents the design and implementation of Vedic multipliers, leveraging ancient Indian mathematics to develop fast, power-efficient multipliers using Ripple Carry Adders (RCA), Carry Select Adders (CSelA), CSelA with Binary to Excess-1 Code (BEC), and CSelA with Common Boolean Logic (CBL). Simulation and synthesis are performed using Cadence tools, showcasing significant improvements in speed, area, and power consumption compared to conventional designs.

Keywords: Vedic Multiplier, Ripple Carry Adder (RCA), Carry Select Adder (CSelA), BEC, CBL, VLSI Design, Cadence Tool.

Introduction

VLSI technology has made remarkable progress in recent years, driving demand for optimized digital circuits with minimal area, delay, and power consumption. One of the critical operations

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in digital circuits is multiplication, which plays an essential role in microprocessors, DSPs, and various data-processing applications. Efficient multiplier design leads to enhanced system performance, particularly in DSP, where convolution and filtering are prominent tasks.

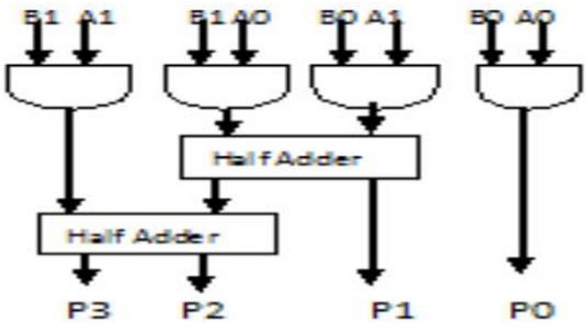

Fig-1. Block diagram of 2 bit Vedic calculator

The Vedic multiplier, inspired by the ancient Urdhva Tiryagbhyam sutra, offers a systematic approach for generating partial products and summing them efficiently. The basic 2x2 Vedic multiplier employs simple AND gates and half adders, forming the building block for higher-order multipliers. Expanding to larger bit multipliers involves hierarchical combinations of these 2x2 units.

Literature Survey

Several adder architectures have been explored to improve multiplier efficiency. Ripple Carry Adders (RCAs) offer simplicity but suffer from long carry propagation delays. Carry Select Adders (CSelA) mitigate this by precomputing results for carry inputs '0' and '1', though at the cost of additional area. Further improvements with BEC and CBL techniques reduce area and power while maintaining high speed.

Prior research indicates that integrating optimized adders within Vedic multiplier architectures yields better performance metrics. Hybrid architectures combining Vedic mathematics and advanced adders promise significant improvements in speed, area, and power efficiency in modern VLSI systems.

ISSN PRINT 2319-1775 Online 2320-7876

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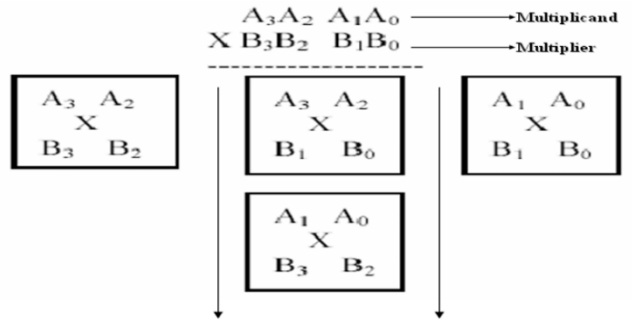

Fig-2 4 Bit Vedic Multiplication Operation.

Proposed System

A. Vedic Multiplier Architecture

The proposed architecture utilizes hierarchical Vedic multipliers constructed from 2x2 blocks. For a 4x4 multiplier, four 2x2 multipliers are combined, generating partial products, which are then summed using optimized adders.

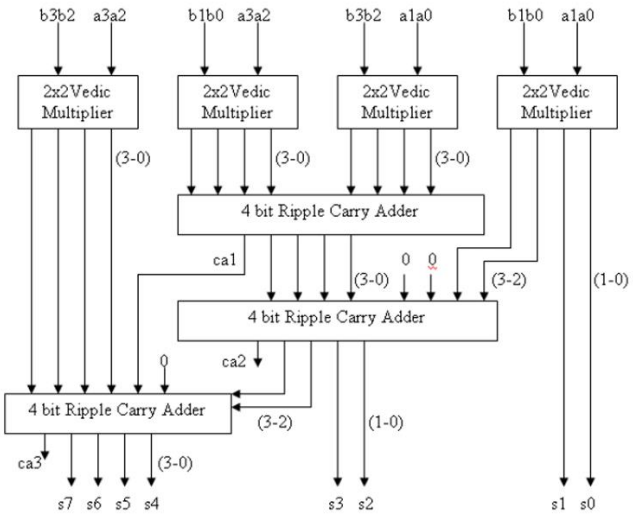

Fig-3 4-bit Vedic Multiplier architecture using RCA

For higher-order designs, such as 8x8 and 16x16 multipliers, the same approach is extended with the addition of efficient adder architectures to manage partial product summation.

B. Adder Topologies

1. Ripple Carry Adder (RCA)

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RCA is the simplest adder structure, where carry propagates sequentially through each full adder. While hardware complexity is minimal, the delay increases with the number of bits due to the ripple effect.

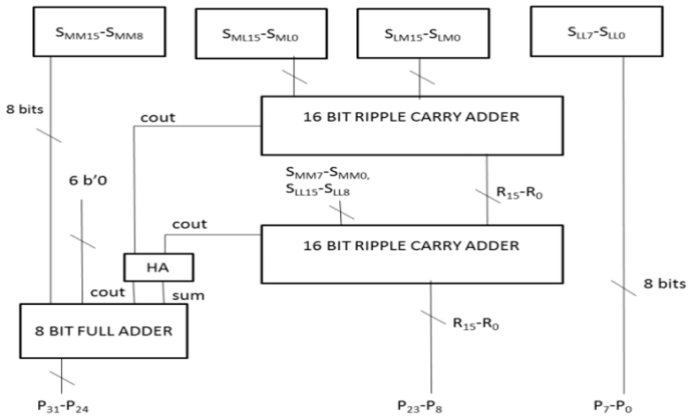

Fig-4 Block Diagram of 16 bit Vedic Multiplier using RCA

2. Carry Select Adder (CSelA)

CSelA reduces propagation delay by computing two sums in parallel, for both possible carry inputs. A multiplexer selects the correct sum once the actual carry is known.

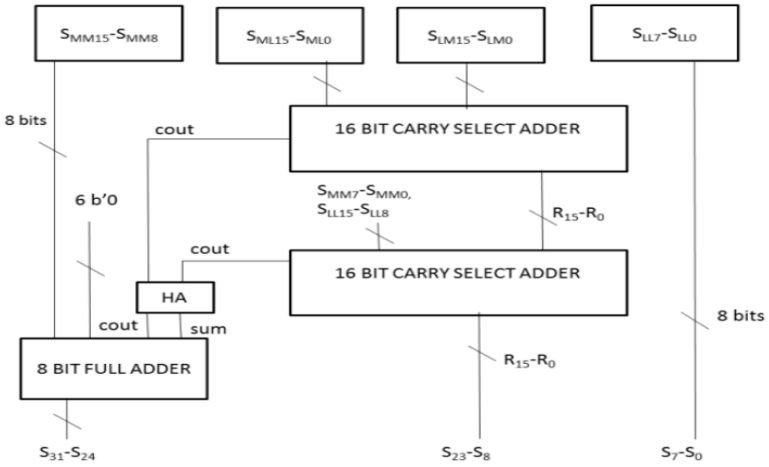

Fig-5 Block Diagram of 16 bit Vedic Multiplier using CSelA

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CSelA with BEC

By replacing one RCA block with a Binary to Excess-1 Code converter, this design reduces redundant logic, saving area and power while maintaining high-speed operation.

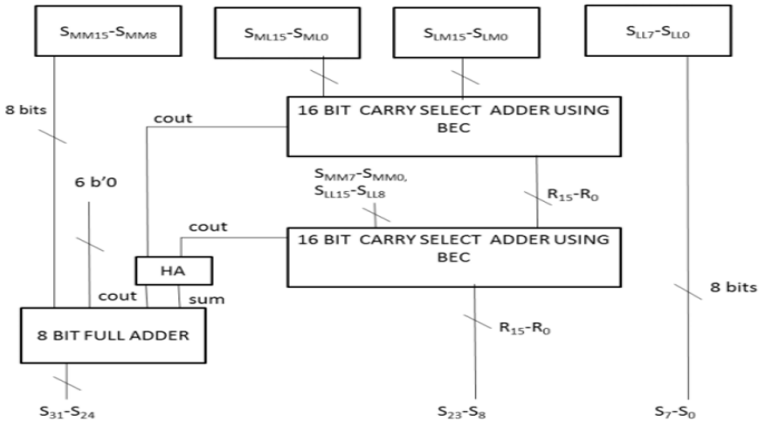

Fig-6 Block Diagram of 16 bit Vedic Multiplier using BEC

CSelA with Common Boolean Logic (CBL)

CBL utilizes optimized Boolean expressions to generate sum and carry outputs, achieving further reduction in area and power without compromising speed.

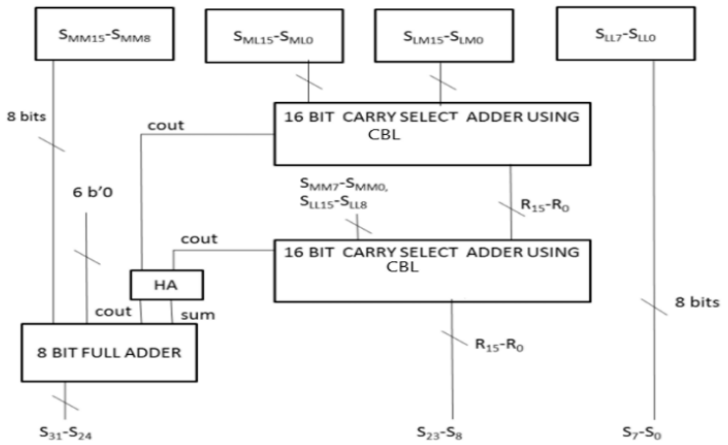

Fig-7 Block Diagram of 16 bit Vedic Multiplier using CBL

Design Flow

The complete design flow of the proposed Vedic multiplier is shown below.

ISSN PRINT 2319-1775 Online 2320-7876

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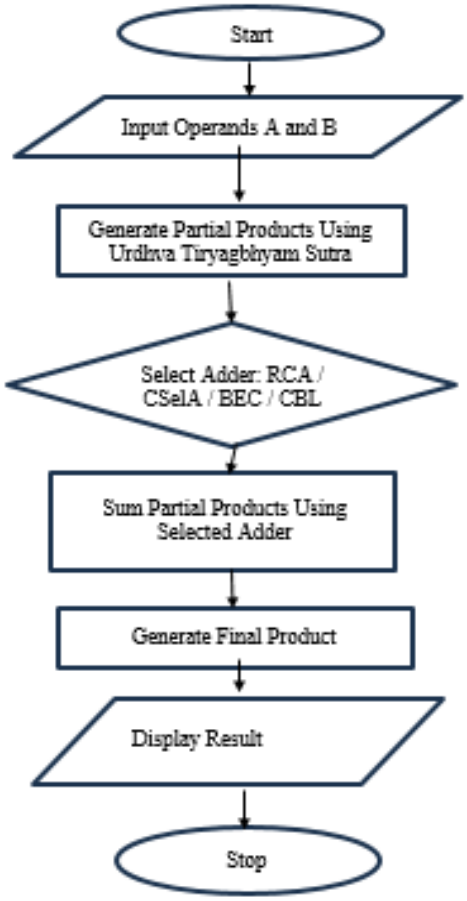

- Start
- Input Operands (A, B)
- Generate Partial Products using Urdhva Tiryagbhyam
- Select Adder Type (RCA / CSelA / BEC / CBL)
- Sum Partial Products
- Output Final Product
- Stop

Implementation Methodology

The proposed architectures are implemented using Verilog HDL. Simulation and functional verification are performed using Cadence NC Verilog. RTL synthesis is conducted in Cadence

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Genus to obtain area, delay, and power reports. Physical implementation, including placement and routing, is carried out in Cadence Innovus.

- Cadence Incisive (NC-Verilog): Functional simulation and verification.
- Cadence Genus: RTL synthesis, generating area, power, and timing reports.
- Cadence Innovus: Placement and routing, ensuring design rule checks and layout generation.

Results and Analysis

A. Simulation Results and Wave Forms

Functional simulation waveforms validate the correctness of the proposed architectures.

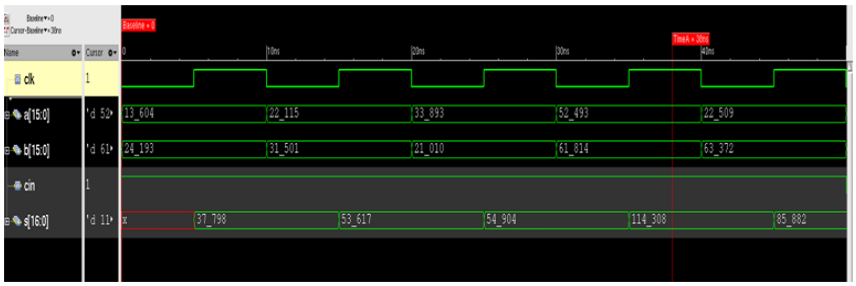

Fig-9 Simulation Waveform of 16 Bit RCA)

The 16-bit Vedic multiplier architecture based on Ripple Carry Adder (RCA) was simulated by applying multiple test vectors. The simulation waveform, as shown in **Fig-9**, demonstrates the accurate computation of the product for given inputs. The design shows correct functionality, with propagation delay corresponding to the nature of the ripple carry structure. As expected, the carry signal ripples through each stage, resulting in increased delay with larger operand sizes.

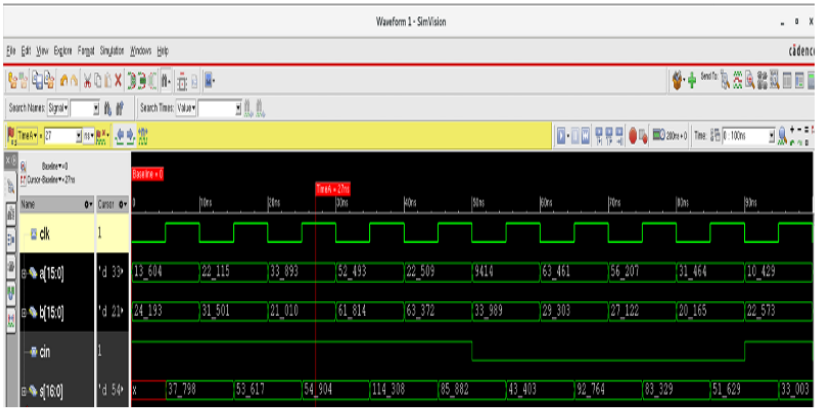

Fig-10 Simulation Waveform of 16 Bit CSelA)

ISSN PRINT 2319-1775 Online 2320-7876

 UGC CARE Listed (Group -I) Journal Volume 11, Iss 2, November 2022

The Carry Select Adder (CSelA) based Vedic multiplier design was simulated to evaluate its improved performance over RCA. As shown in **Fig-10**, the simulation waveform highlights reduced propagation delay due to parallel generation of sums for different carry inputs. The multiplexer selects the appropriate result once the actual carry is determined. This leads to faster computation with accurate outputs for all tested input combinations.

Fig-11 Simulation Waveform of 16 Bit CSelA using BEC)

The CSelA with Binary to Excess-1 Code (BEC) converter offers an optimized solution, minimizing hardware usage while maintaining speed. The simulation waveform in Fig-11 validates the correct output generation with further reduced area and power consumption compared to CSelA alone. The design successfully computes the product in less time, as evidenced by the faster transition and stable output values across multiple input vectors.

Synthesis Reports

Post-synthesis analysis provides insights into the area, delay, and power consumption of each architecture.

Architecture	Area (mm^2)	Delay (ns)	Power (nW)
RCA (16-bit)	378.274	3.90	108.738e-05
CSelA (16-bit)	374.465	3.456	98.7325e-05
CSelA with BEC (16-bit)	370.212	3.210	92.4783e-05
CSelA with CBL (16-bit)	368.150	3.105	89.3451e-05

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Conclusion and Future Scope

Conclusion

The paper presents an efficient Vedic multiplier design using various optimized adder topologies. Among the architectures explored, CSelA with CBL demonstrates the best performance in terms of area, power, and delay. The integration of Vedic mathematics with advanced adder designs significantly enhances multiplier efficiency for VLSI applications.

Future Scope

Future work can focus on:

- Extending the design to 32-bit and 64-bit multipliers.
- Exploring advanced adders like parallel prefix adders.
- Implementing real-time applications on FPGA platforms.
- Developing adaptive multipliers based on workload demands.
- Combining multi-modal optimization strategies for ultra-low power applications.

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