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DESIGN A HIGH SPEED MULTIPLIER USING AHL LOGIC WITH RAZOR FLIP

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Abstract: In most digital signal processors, multipliers serve as crucial components, significantly impacting system performance based on their throughput. In modern technology nodes, reliability has become a critical design consideration. Transistor aging adversely affects system performance over time, potentially leading to delay-related failures, with the impact of aging intensifying as transistor size scales down. Bias Temperature Instability (BTI) is a primary cause of transistor aging, leading to an increase in threshold voltage over time and a consequent reduction in multiplier speed. Although over-design approaches can mitigate aging effects, they often result in power and area inefficiencies. Fixed latency designs are prone to timing violations, making variable latency multipliers preferable for reliable operation under BTI effects. Adaptive Hold Logic (AHL) is utilized to appropriately select the cycle period, while an Error Detection and Correction Pulsed Latch (ECPL) is employed to detect timing errors.

Keywords: Digital Signal Processor, Bias Temperature Instability (BTI), Adaptive Hold Logic (AHL), Error Detection and Correction Pulsed Latch (ECPL)

I. INTRODUCTION

Typical DSP applications such as fourier transform, discrete cosine transforms and digital filtering, where multipliers play an important role. Multipliers are complex circuits and it operates at a high clock rate. So to obtain a satisfactory performance the delay of the multiplier should be minimum. The re-liability degradation of the circuit is a critical issue in nanometer technologies. One of the main reason for performance degradation in nano scale circuits is Bias Temperature Instability (BTI). PMOS transistors operating with negative gate to source voltage face Negative Bias Temperature Instability (NBTI). Due to this effect, threshold voltage Vth increases with time. So the performance of the system reduces over time. The similar effect in NMOS transistor is Positive Bias Temperature Instability (PBTI). These effects may cause timing violations in multiplier with time and it effects the whole system. Hence, a reliable multiplier design is essential to obtain satisfactory performance.

For the proper performance of the system, critical path delay is used as system clock cycle in traditional circuits and it may cause significant timing wastage. The timing wastage in traditional circuits can be minimized by incorporating variable latency

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design in the system. In variable latency design, the circuit contains two paths: a shorter path and a longer path. Shorter path can execute the operation correctly in one cycle and longer path can execute the operation correctly in two cycles [1].

The most widely used arithmetic functional units in numerous applications such as the discrete Fourier transform, fast fourier transform etc. and digital filtering techniques are called as digital multipliers. The throughput performance of entire circuits will be diminished, if the multipliers are consuming long time duration. The delay of multipliers can be attributed to the delay of adders as multiplication is a sequence of addition process.

Adders are a critical hardware unit for the efficient implementation of multiplier unit. Adder can be applied in majority of applications. Adders are playing a vital role in arithmetic logic unit as well as other parts of the processor. Addition operation can also be used in operations of complement, encoding, decoding and the like. Generally, process of addition involves two or more numbers which are added and whose carry is generated. The output of addition operations will give the sum and carry value. All complex adder architectures are constructed from the basic building blocks which are 2 bit Adder (HA) as well as 3 bit Adder (FA). Hence the delay produced in an adder would be reflected in the multiplier and this would in turn be mirrored as degradation of performance of the entire circuit. This is termed as transistor aging [2].

II. LITERATURE SURVEY

M. Sathyamoorthy, B. Sivasankari, P. Poongodi et. al. High speed and low Power consumption is one of the most important design objectives in integrated circuits. As multipliers are the most widely used components in such circuits, the multipliers must be design efficiently. This paper proposes the simple and efficient approach to reduce the maximum power consumption and delay. Based on the idea of razor flip flop and adaptive hold logic the timing violations are reduced. In the fixed latency usage of clock cycles is increased. The reexecution of clock cycles is reduced by using variable latency. The result analysis shows that the reliable multiplier has better performance in power consumption and delay than contemporary architectures [3].

V. S. Chirde and U. Jadhav et. al. In VLSI, transistor scaling plays an important role in reducing the power dissipation and increasing speed from one technology node to another technology node. But transistors are scaled further in size then it will lead to number of limitations like short channel effect, sub-threshold condition, body effect, aging effects etc. Negative Bias Temperature Instability (NBTI) is increase in threshold voltage (Vth) when pMOS transistors are under negative bias (Vgs=-Vdd). This effect reduces the speed of the circuit. In this paper, a design of a multiplier with Adaptive Hold Logic (AHL) circuit is proposed to reduce Aging Effects. The Adaptive Hold Logic (AHL) circuit is used to indicate the aging effects of transistor.

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The circuit is designed in Tanner EDA (Electronic Design and Automation) 13.0 tool with 22-nm technology node [4].

F. Van De Putte and C. Straßer et. al. A broad range of defeasible reasoning forms has been explicated by prioritized adaptive logics. However, the relative lack in meta-theory of many of these logics stands in sharp contrast to the frequency of their application. This article presents the first comparative study of a large group of prioritized adaptive logics. Three formats of such logics are discussed: superpositions of adaptive logics, hierarchic adaptive logics from F. Van De Putte (2011, Log. J. IGPL, doi:10.1093/jigpal/jzr025) and lexicographic adaptive logics from F. Van De Putte and C. Straßer (2012, Log. Anal., forthcoming). We restrict the scope to logics that use the strategy Minimal Abnormality. It is shown that the semantic characterizations of these systems are equivalent and that they are all sound with respect to either of these characterizations. Furthermore, sufficient conditions for the completeness and equivalence of the consequence relations of the three formats are established. Some attractive properties, including Fixed Point and the Deduction Theorem, are shown to hold whenever these conditions are obeyed. [5].

I. -C. Lin, Y. -H. Cho and Y. -M. Yang et. al. Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (V gs = -V dd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a columnor row-bypassing multiplier. The experimental results show that our proposed architecture with 16 × 16 and 32 × 32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column-bypassing multipliers. Furthermore, our proposed architecture with 16 × 16 and 32 × 32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement as compared with 16×16 and 32 × 32 fixed-latency row-bypassing multipliers [6].

P. K. Parveen and C. Priya et. al. Present day technology uses many types of multipliers such as Array multiplier, Column and Row Bypassing multiplier. Those multipliers consume more power and occupyan extra area because of its number of blocks. Reducing power dissipation is one

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of the most critical issues in very large scale integration design today. A sub threshold leakage current plays a dominant role in power dissipation. To rectify this difficulty those multipliers are replaced with Vedic multiplier. The Vedic multiplier with AHL circuit helps to increase the performance of the multiplier. Vedic multiplication reduces computation time by Urdhva - tiryakbhyam sutra of Vedic mathematics. Vedic multiplier is efficient in silicon area per speed. It occupies less area because of its reduced number of logic blocks. But in this multiplier the power is dissipated in both active and standby modes. MTCMOS is used to overcome this problem. Multi-threshold technology is a noteworthy technique to reduce leakage power. MTCMOS logic is effective in standby leakage control technique, which is used to adjust the threshold voltage of the circuit. The multiplier is designed with 8×8 bit Vedic multiplier with MTCMOS logic. It makes the circuit as the low leakage circuit and also used to reduce the power and delay of the circuit. It makes the circuit as the low power and high performance circuit [7].

M. V. Archana and K. E. Suresh et. al. In most of the digital signal processors, multiplier is used as a key component. So, the performance of the system depends on the throughput of the multiplier. Now a days, reliability is an important design concern in advanced technology nodes. Performance of the system is significantly affected by the aging of transistor and the system may fail due to delay problems in long term. The impact of aging getting higher with the scaling of transistor. One of the main cause for aging in transistor is Bi-as Temperature Instability (BTI). Due to this effect threshold voltage of the transistor increases over time and it reduces the multiplier speed. Over-design approaches can be used to reduce the aging effect, but these may cause power and area inefficiency. Fixed latency designs have high chance of timing violations. So, a multiplier with variable latency is used for reliable operation under BTI effects. An Adaptive Hold Logic (AHL) is used for the proper selection of cycle period and an Error Detection Correction Pulsed Latch (ECPL) is used for the detection of timing errors [8].

III. METHODOLOGY

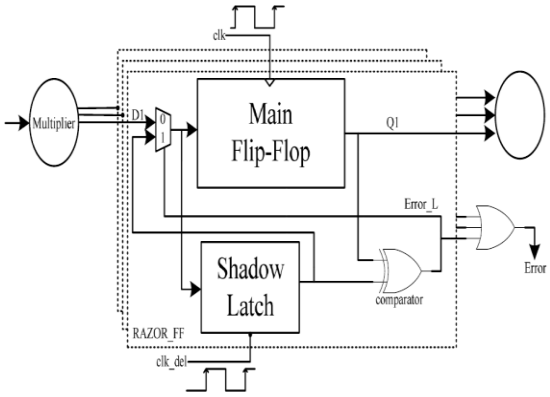

Fig. 1: Razor flip flops

Fig. 1 shows the details of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current

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operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to re-execute the operation and notify the AHL circuit that an error has occurred.

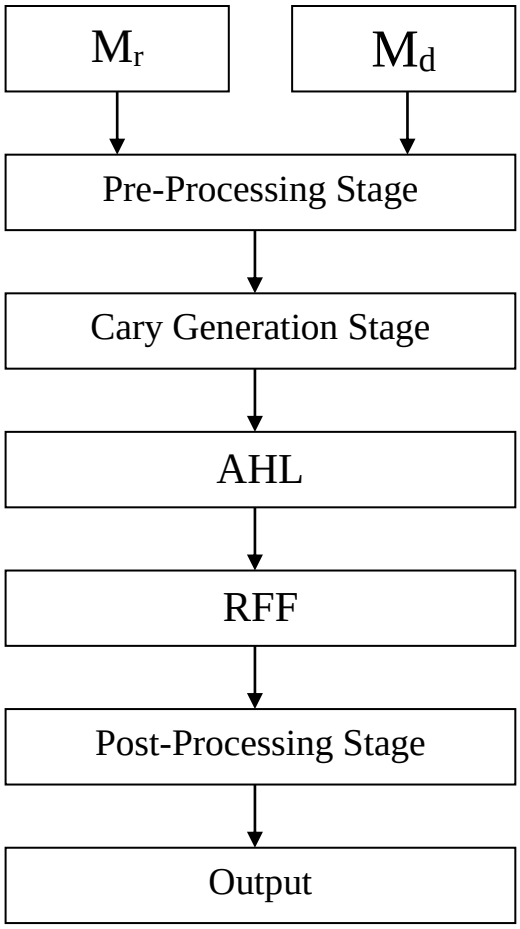

Fig. 2: Block Diagram

We use Razor flip-flops to detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is re-executed with two cycles. Although the re-execution may seem costly, the overall cost is low because the re-execution frequency is low.

Carry generation is a fundamental concept in digital electronics, particularly in the design of arithmetic circuits like adders. It refers to the process of determining whether a carry-out will be generated from a given bit position in a binary addition operation. This is essential for efficient multi-bit addition, where the carry-out from one bit needs to be propagated to the next higher bit position. In full adders and more complex structures like carry-look ahead adders, carry generation helps speed up the addition process by quickly resolving carry dependencies, thus improving overall computational speed.

Adaptive Hold Logic (AHL) is a technique used in digital circuit design to optimize performance and power consumption, particularly in pipelined processors and memory systems. AHL dynamically adjusts the clock cycle or delay times based on the varying workload and operating conditions. By intelligently managing the hold times, AHL ensures that data is correctly processed and latched without unnecessary delays, improving overall efficiency. This adaptive approach helps in balancing the trade-off between speed and reliability, making the system more resilient to variations in voltage, temperature, and process parameters.

A Razor flip-flop is an advanced type of flip-flop used in digital circuits to detect and correct timing errors, enhancing the reliability and performance of high-speed processors. It integrates error-detection mechanisms that monitor the timing of data transitions. If a timing violation occurs, the Razor flip-flop captures the erroneous data and signals a correction mechanism,

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allowing the system to recover gracefully. This approach allows for aggressive clocking, pushing the performance limits of processors while maintaining data integrity and reducing power consumption.

Post-processing refers to the series of actions taken to refine and enhance data or outputs after the initial processing stage. In various fields, this can include activities such as filtering noise from audio recordings, color correction in photography, rendering in computer graphics, or smoothing data in scientific analysis. The goal of post-processing is to improve the quality, usability, and presentation of the results, ensuring they meet desired standards and are ready for final use or publication. This step is crucial for achieving high-quality outcomes and addressing any deficiencies from earlier stages of processing.

IV. RESULTS

In Fig.2 shows the accuracy comparison graph is observed between existing system and proposed system. The proposed system shows the high accuracy.

In Fig.3 shows the precision comparison graph is observed between existing system and proposed system. The proposed system shows the high precision.

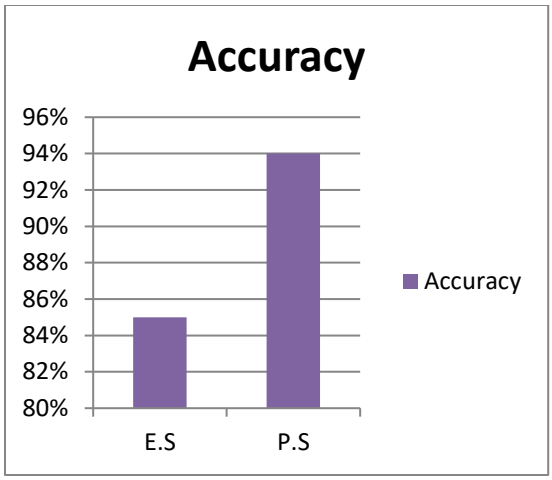

Fig. 2: Accuracy Comparison Graph

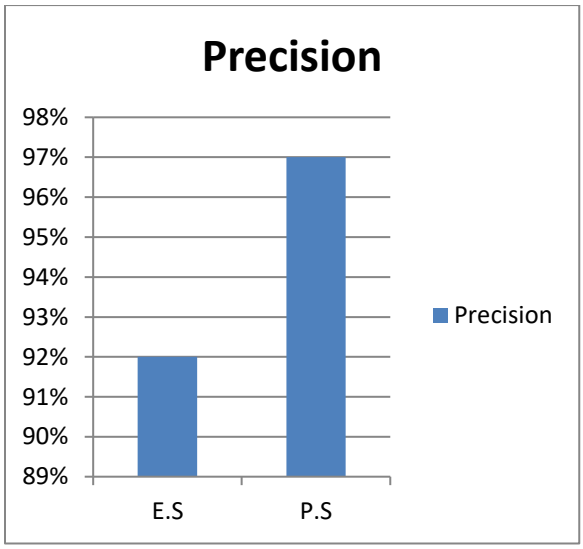

Fig. 3: Precision Comparison Graph

V. CONCLUSION

Multipliers are vital in digital signal processors, with their performance heavily influencing overall system throughput. As technology advances, ensuring reliability amidst transistor aging, particularly due to Bias Temperature Instability (BTI), has become increasingly critical. BTI induces threshold voltage shifts, diminishing multiplier speed and potentially causing delay-related failures. While over-design

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can counteract aging effects, it often leads to inefficiencies in power and area utilization. To address these challenges, variable latency multipliers, which adapt to BTI-induced changes, offer a more reliable solution compared to fixed latency designs. Employing Adaptive Hold Logic (AHL) to dynamically adjust cycle periods and integrating Error Detection and Correction Pulsed Latch (ECPL) for timing error detection ensures robust operation and extends the lifespan of multipliers in modern digital signal processors. This approach balances performance, power efficiency, and reliability, meeting the demands of evolving technology nodes. Hence, this analysis achieves better results in terms of accuracy and precision.

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